High-precision Real Time Clock circuit with thermal compensation and built-in quartz resonator

(Functional analogue of RX8025SA by Company « Epson Toyocom »)

The IZ1325 high-precision real-time clock circuit with thermal compensation and built-in quartz resonator, provides high accuracy counting the current time of the, generation of 6 system interruptions and two independent event signals. The device provides both 24/12-hour operation modes and contains the built-in supply control circuit, frequency adjustment circuit for high accuracy of the system generator. The IZ1325 support data and command exchange by means of standard 2-wire interface (I^2C-bus).

The IC is applied in the wide range of the industrial and household equipment and appliances, where it is required to counting and processing of the system current time data.

Main functions:

- seconds, minites hours, weekday, date, month and year time counting;
- two operational modes12/24-hours;
- data and command exchange via 2-wire I^2C-bus serial interface;
- 6 system interrupts generation;
- 2 independent alarms: day, hours, minutes and hours, minutes;
- supply voltage and system generator frequency monitoring.

Main features:

- Supply voltage, U_{DD}, 1,7 … 5,5 V
- Oscilator operating supply voltage U_{CLK}, 1,15 … 5,5 V
- Operating temperature range -40 to +85 °C

Table 1 – Contact pad description

Contact pad number	Symbol	Description
01	GND	Ground
02	INTA	Interrupt output A
03	X1	Quartz resonator input
04	X2	Quartz resonator output
05	FOE	Control input
06	V_{DD}	Power supply
07	TEST	Test terminal
08	FOUT	32.768 kHz clock output
09	SCL	I^2C bus clock input
10	SDA	I^2C bus input-output
11	INTB	Interrupt output B

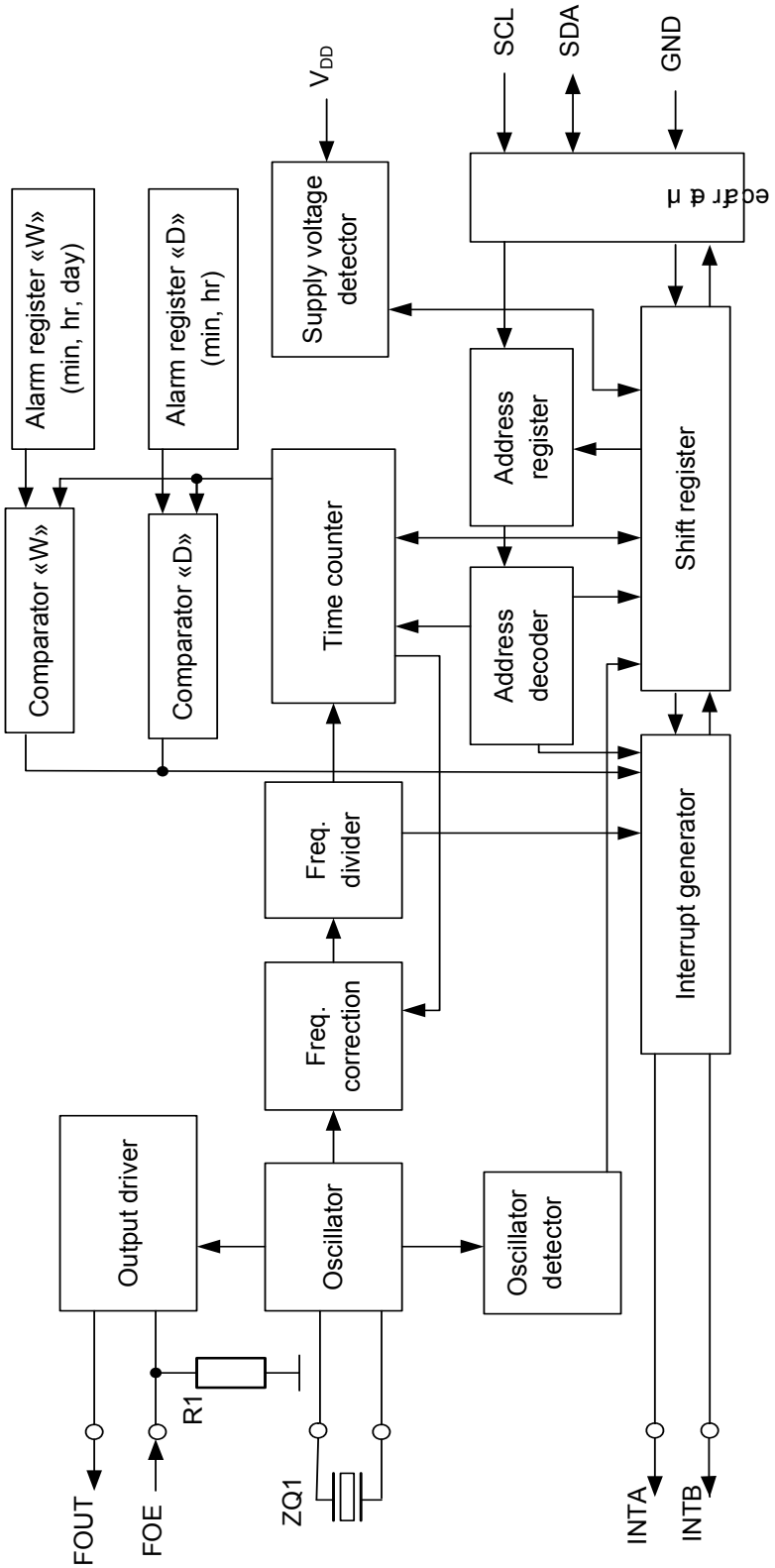


Fig. 1 – Block-diagramm

Table 2 – Maximum ratings

Symbol	Parameter	Targets		Unit
		Min.	Max.	
U_{DD}	Supply voltage	-0,3	6,5	V
U_I	SCL, SDA and FOE pins input voltage	-0,3	6,5	V
U_{01}	SDA, INTA and INTB pins output voltage	-0,3	6,5	V
U_{02}	FOUT pin output voltage	-0,3	U_{DD}+0,3	V
U_{IH}	Input high voltage	-	6,5	V
U_{IL}	Input low voltage	– 0,3	-	V

Table 3 – Recommended operating condition

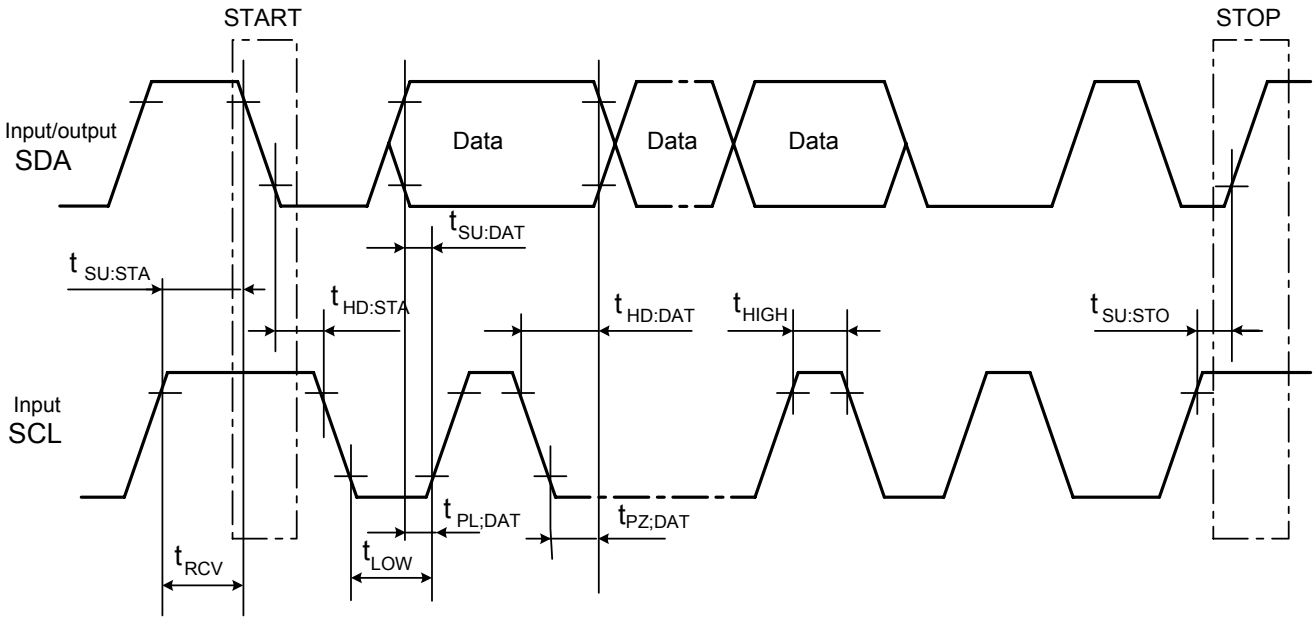
Symbol	Parameter	Targets		Unit
		Min.	Max.	
U_{DD}	Supply voltage	1,7	5,5	V
U_I	SCL, SDA and FOE pins input voltage	– 0,3	5,5	V
U_{01}	SDA, INTA and INTB pins output voltage	– 0,3	5,5	V
U_{02}	FOUT pin output voltage	-0,3	U_{DD}	V
U_{IH}	Input high voltage	0,8U_{DD}	5,5	V
U_{IL}	Input low voltage	0	0.2 U_{DD}	V
f_{SCL}	Input clock frequency - SCL input	-	400	kHz
U_{CLK}	Oscilator supply voltage	1,15	5,5	V

Table 4 – Electric parameters

Parameter, unit	Symbol	Mode of measurements	Targets		Ambient temperature, °C
			Min	Max	
Output high current, mA	I_{OH}	Pin FOUT U_{OH}= U_{DD}-0,5 U_{DD} = 3 V	-	-0,5	25±10 85 -40
Output low current, mA	I_{OL1}	Pin FOUT U_{OL} = 0,4 V U_{DD} = 3 V	0,5	–	
	I_{OL2}	Pins INTA, INTB U_{OL} = 0,4 V U_{DD} = 3 V	1,0	–	
	I_{OL3}	Pin SDA U_{OL} = 0,4 V U_{DD} = 3 V	4,0	–	
Input leakage current, μA	I_I	Pin SCL U_{DD} = 5,5 V U_I = 0 V U_I = 5,5 V	-	|±1,0|	
Input current, μA	I_{IFOE}	Pin FOE U_{DD} = 5,5 V	–	1,0	
OFF-state output current, μA	I_{OZ}	Pins SDA, INTA, INTB U_{DD} = 5,5 V U_O = 0 V U_O = 5,5 V	–	|±1,0|	
Dynamic consumption current, μA	I_{DDS1}	U_{DD} = 3,0 V	–		
	I_{DDS2}	U_{DD} = 5,0 V	–	1,8	
Consumption current, μA	I_{DD}	U_{DD} = 5,5 V f_{FOUT} = 32,768 kHz	–	6,5	

Table 5 – Typical values of electric parameters Ta = 25 °C

Parameter, unit	Symbol	Mode of measurements	Typical value[1)]
Dynamic consumption current, μA	I_{DDS1}	f_{SCL}= 0 Hz, pin FOUT not connected, without load, 0 V applied to pin FOE, 3,0 V applied to pins INTA, INTB, V_{DD}	0,48
Frequency deviation, $\times10^{-6}$	Δf/f	U_{DD} = 3,0 V	±5
Frequency voltage characteristic, $\times10^{-6}$/B	Δf/V	U_{DD} = 2,0 … 5,0 V	±1
Frequency temperature characteristic, $\times10^{-6}$	Δf_{TOP}	U_{DD} = 3,0 V	from -120 to +10
Oscilator start-up time, s	t_{STA}	U_{DD} = 2,0 V	not more 1
[1)] Typical value is arithmetic mean of parameter value, of measured sampling			



START condition hold time $t_{HD:STA} \geq 0{,}6\ \mu s$.
SCL low time $t_{LOW} \geq 1{,}3\ \mu s$.
SCL high time $t_{HIGH} \geq 0{,}6\ \mu s$.
START condition set-up time $t_{SU:STA} \geq 0{,}6\ \mu s$.
Data hold time $t_{HD:DAT} \geq 0$ ns.
Data set-up $t_{SU:DAT} \geq 200$ ns.
SCL fall to SDA low delay $t_{PL\ DAT} \leq 900$ ns.
SCL fall to SDA third state delay $t_{PZ:DAT} \leq 900$ ns.
STOP condition set-up time $t_{SU:STO} \geq 0{,}6\ \mu s$.
STOP to START condition recovery time $t_{RCV} \geq 62\ \mu s$.

Fig. 3 –Timing diagram of data transfer

Operation

IZ1325 operates on the serial bus as the «slave» device. START condition has to be set-up , register address and device identification code has to transferred the to get access to the device. The next registers can be addressed in series till the condition STOP is set-up. When supply voltage drops below 1,8 V, access to the device by the serial interface is not guaranteed. The current time is counted with the supply voltage 1 ÷ 5,5 V.

Time and date reading is performed by means of reading of the appropriate register bytes. Set-up and initialization of the time and calendars performed by means of data writing to the appropriate bytes. Data, contained in the time, calendar and alarm registers is coded in BCD format.

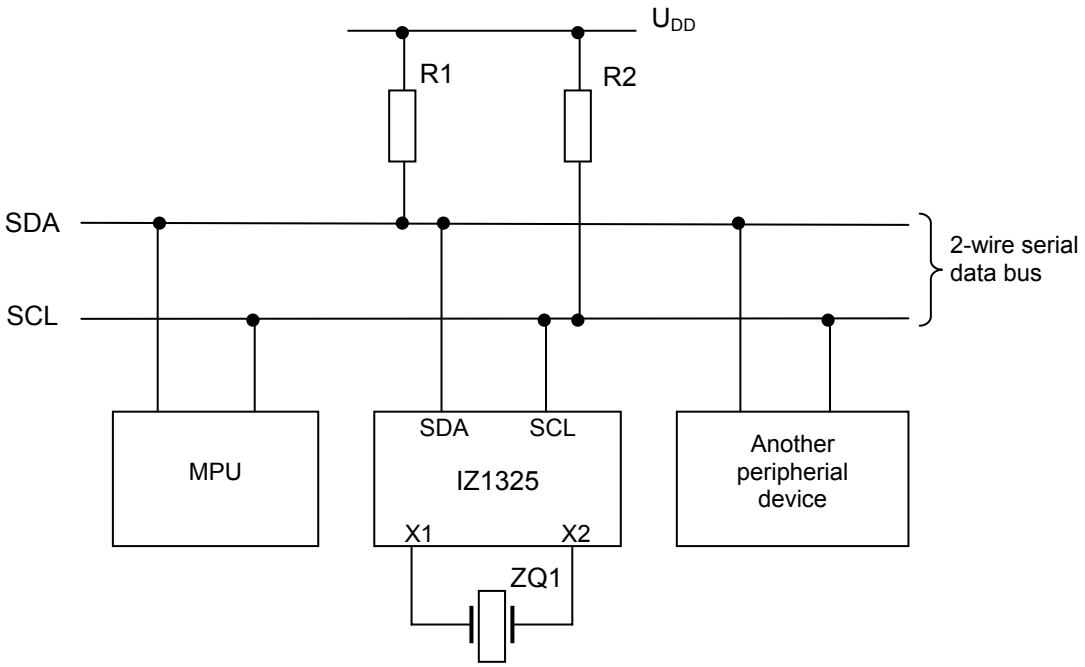
After START condition issued to 2-wire bus the data on current time transferred from counters to the set of auxiliary registers. The data on time are read out from these auxiliary registers, while the watch continue to operate. This eliminates the need in the repeated reading in case of updating the basic registers during the access process.

Table 6 – Structure of RTC registers

Address	Data								RTC registers
	D7	D6	D5	D4	D3	D2	D1	D0	
0	-	S40	S20	S10	S8	S4	S2	S1	Seconds
1	-	M40	M20	M10	M8	M4	M2	M1	Minutes
2	-	-	H20 P,/ A	H10	H8	H4	H2	H1	Hours
3	-	-	-	-	-	W4	W2	W1	Weeks
4	-	-	D20	D10	D8	D4	D2	D1	Weekdays
5	-	-	-	MO10	MO8	MO4	MO2	MO1	Monthes
6	Y80	Y40	Y20	Y10	Y8	Y4	Y2	Y1	Years
7	-	F6	F5	F4	F3	F2	F1	F0	Digital adjustment
8	-	WM40	WM20	WM10	WM8	WM4	WM2	WM1	Alarm 1: minutes
9	-	-	WH20 WP,/A	WH10	WH8	WH4	WH2	WH1	Alarm 1: hours
A	-	WW6	WW5	WW4	WW3	WW2	WW1	WW0	Alarm 1: weekdays
B	-	DM40	DM20	DM10	DM8	DM4	DM2	DM1	Alarm 1: minutes
C	-	-	DH20 DP,/A	DH10	DH8	DH4	DH2	DH1	Alarm 1: hours
D	Not used								Not used
E	WALE	DALE	/12, 24	/CLEAN2	TEST	CT2	CT1	CT0	Control 1
F	VDSL	VDET	/XST	PON	/CLEAN1	CTFG	WAFG	DAFG	Control 2

2- Wire Serial Data Bus

IZ1325 supports the bi-directional 2-wire bus and the data transfer protocol. The bus can be controlled by the “master” device, which generates the clock signal SCL, controls access to the bus, generates the conditions START and STOP.



ZQ1 – quartz resonator C-002RX or C-004R from «Epson Toyocom», Japan
R1, R2 – resistors (R1 = R2)

Fig. 4 – Typical configuration of 2- wire bus

Data transfer can be started only when the bus is not busy. In the process of the data transfer, the data line should remain stable, while the clock line is HIGH. Transition of the data line, while the clock is HIGH will be interpreted as control signals.

START and STOP conditions

A HIGH-to-LOW transition of the data line, while the clock line is HIGH, is defined as the START condition (Data transfer start)

A LOW-to-HIGH transition of the data line while the clock line is HIGH is defined as the STOP condition (Data transfer stop).

A HIGH-to-LOW transition of the data line, while the clock line is HIGH, is defined as the RESTART condition (Repeated start condition)

STOP to START condition recovery time $t_{RCV} \geq 62$ μs.

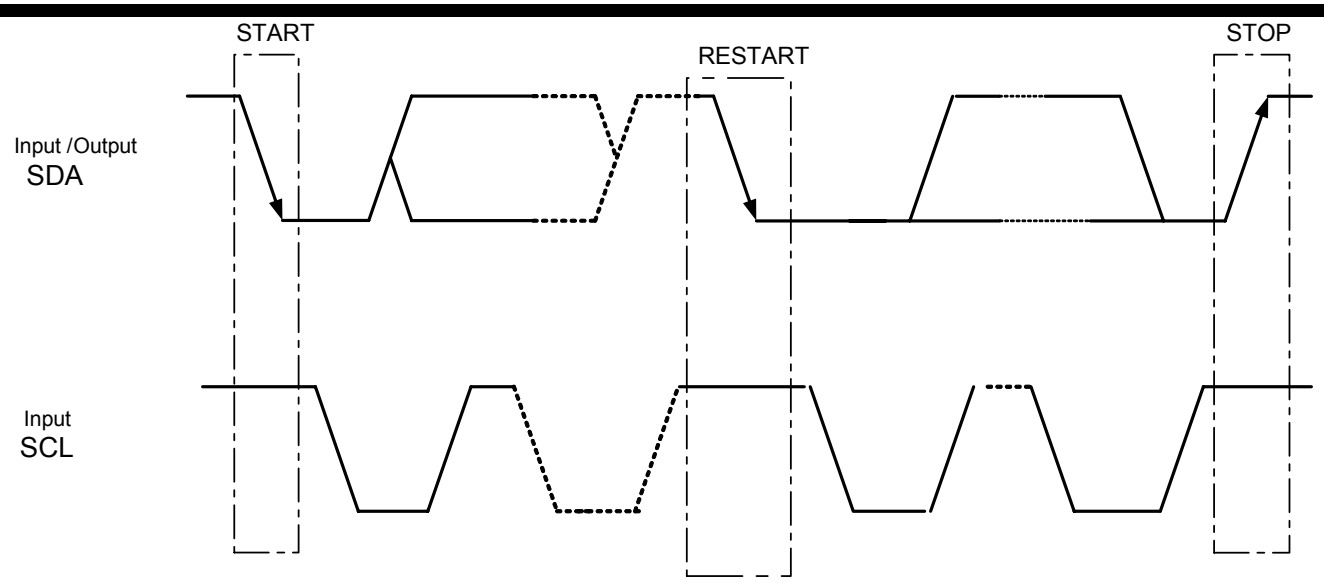


Fig. 5 –START and STOP conditions

Data transfer and reception acknowledge

Each data transfer starts with START condition and ceases with STOP condition. The number of data bytes, transferred between the START and STOP conditions, is not limited and is specified by the «master» device. (but, the transfer time should not exceed 0,5s) Data is transferred byte by byte, and each byte reception is confirmed by the ninth (acknowledge) bit.

Data line state corresponds to the valid data, if after the condition START the data line remain stable during the HIGH period of the clock pulse. Changes of the data line have to be performed during the LOW period of the clock pulse. One data bit is transferred during each clock pulse.

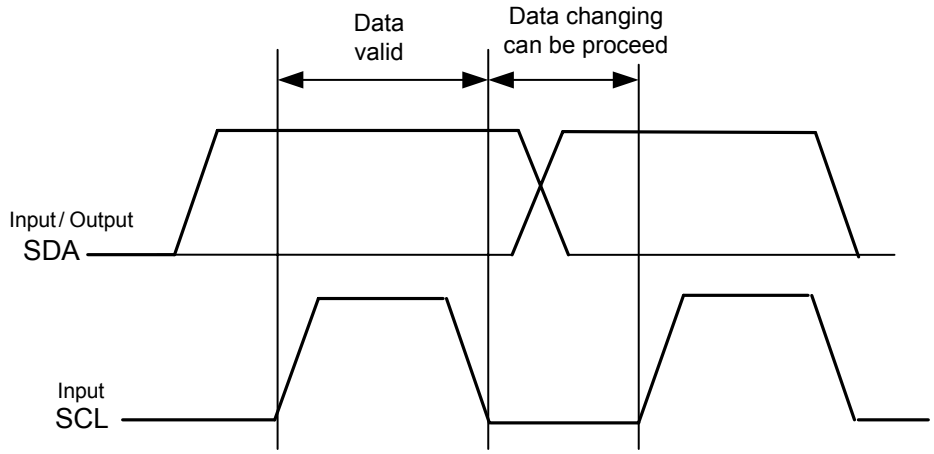


Fig. 6 –Data transfer

Each receiving device being addressed, generates the reception acknowledge bit after reception of each byte. The «master» device should generate the additional clock pulses, which are set in compliance with the acknowledge bits.

If the reception acknowledge signal is HIGH, then on the acknowledge clock pulse, confirming reception, the device should switch the SDA line to LOW. Set-up time and the hold time should be taken into consideration. The «master» device should signal about termination of the data transfer to the «slave» device, stopping generation of the acknowledge bit, while receiving from the «slave» clock pulse of the reception acknowledge. In this case, the «slave» clock pulse should switch the data line to LOW to permit to the «master» to generate the STOP condition.

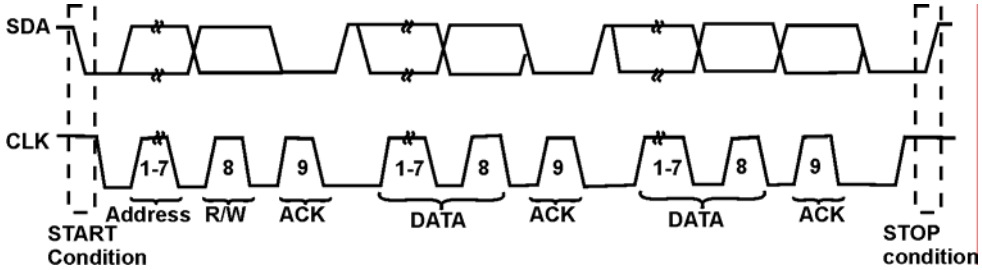


Fig. 7 –Data transfer

Depending on the status of the bit $R/\overline{W}$, two types of transfer are possible:

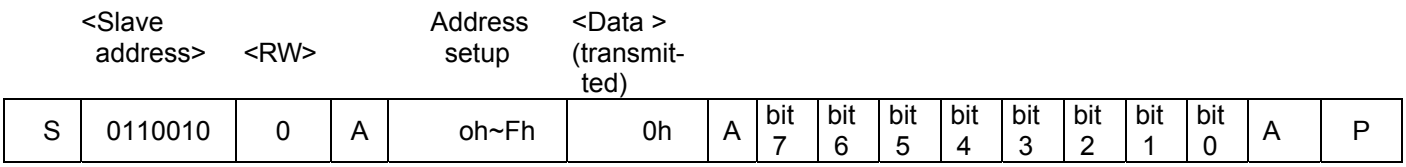
- Data transferred from the «master» transmiter to the «slave» receiver. The first byte, transferred by the «master», is the address of the «slave» device. Then follows sequence of the data bytes. The «slave» one returns the reception acknowledge bits after each received byte. Order of the data transfer: the first one is the most senior digit (MSB).

- Data are transferred from the «slave» transmiter to the «master» receiver. The first byte (address of «slave») is transferred to the «master». Then the «master» returns the acknowledge bit. This follows by data sequence transmission by «slave». The «master» device returns the reception confirmation bit after each received byte, with exception of the last byte. After reception of the last byte the reception confirmation bit does not return.

The «master» device generates all clock pulses and the conditions START and STOP. Transmission completes with generation of the STOP condition or the repeated generation of the START condition. As the repeated START condition is the beginning of the next serial transmission, then the bus is not vacated. Data transfer order: the first one is the most senior digit (MSB).

Read-out mode

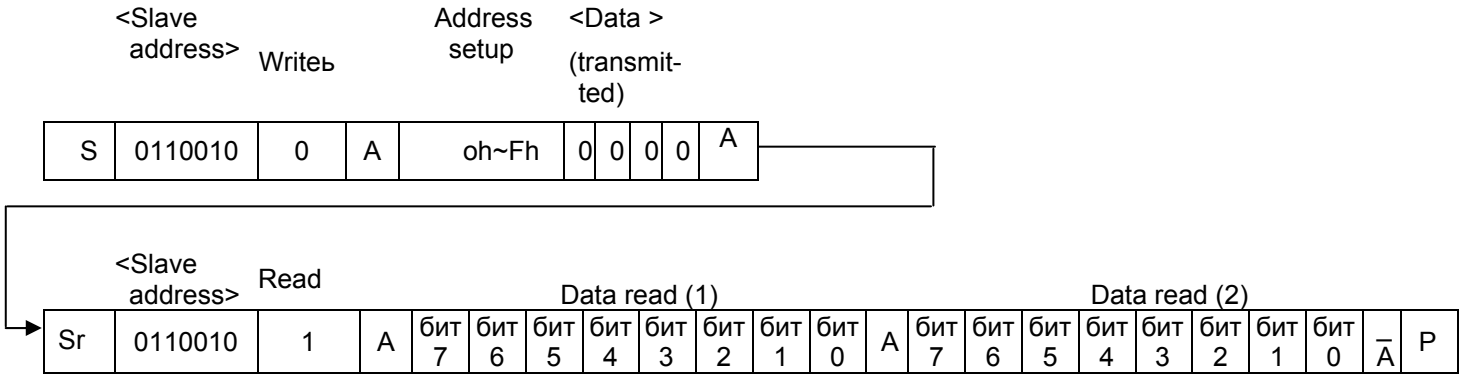
After transmission of each byte the confirming bit is transferred. Conditions START and STOP are interpreted as the start and end of the serial transmission. Addressing is performed by the hardware means after reception of the address of the «slave» device and the direction bit. The address byte is the first byte, received after the START condition, generated by the «master» device. Address byte contains seven address bits IZ1325, equal to «0110010», accompanied by the direction bit ($R/\overline{W}$), which is equal to “0” for writing. On receiving and decoding the address IZ1325 generates acknowledge on the line SDA. After acknowledge of the «slave» address and the write bit, the «master» device transmits the register address of IZ1325. Thus, the register indicator will be set in IZ1325. Then the «master» device will start to transmit each data byte with the subsequent acknowledge of receiving of each byte received. Upon completion of writing the «master» one will generate the STOP condition, for termination of the data transfer.



S – START condition
A – Acknowledged receiving
P – STOP condition

Fig. 6 – Data write mode

Data read mode



S – START condition
A – Acknowledged receiving
P – STOP condition
Sr – RESTART condition
Ā –Not acknowledged receiving

Fig. 7 – Data read mode

The first byte is received and is processed as in the mode of the «slave» receiver. But in this mode the direction bit will indicate, that the transmission direction is changed. The serial data are transmitted by IZ1325 by means of SDA, the clock pulses – by means of SCL. The START and STOP conditions are interpreted as the start and end of serial transmission. The address byte is the first byte, received after START condition, generated by the «slave» device. The address byte contains the seven address bits, equal to «0110010», accompanied with the direction bit ($R/\overline{W}$), which is equal to “1” for reading. After receiving and decoding the address byte IZ1325 accepts confirmation from the line SDA. Then IZ1325 starts to transmit the data from the address, indicated by address register. If the address register is not written before initialization of the reading mode, then the first read address will be the last address, stored in the register indicator. IN8563 should transmit the bit of «non-acknowledge», in order to finish reading.

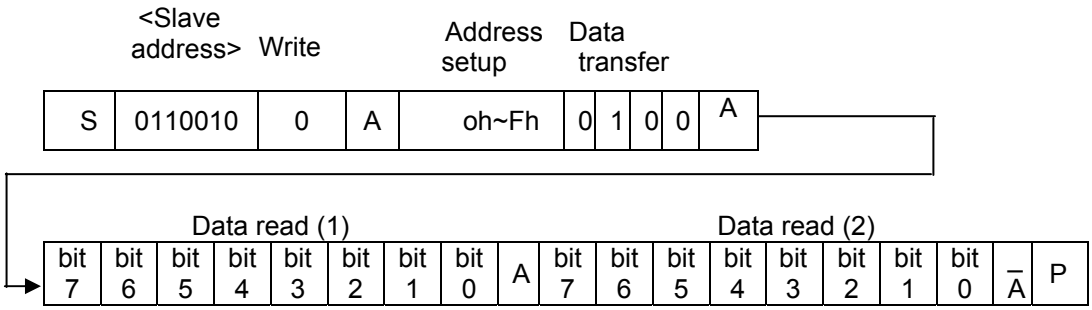


Fig. 8 – Simplified algorithm of data reading

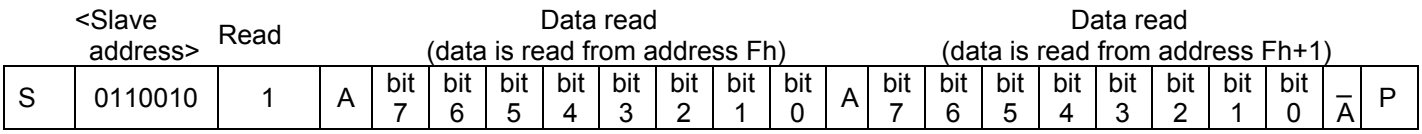
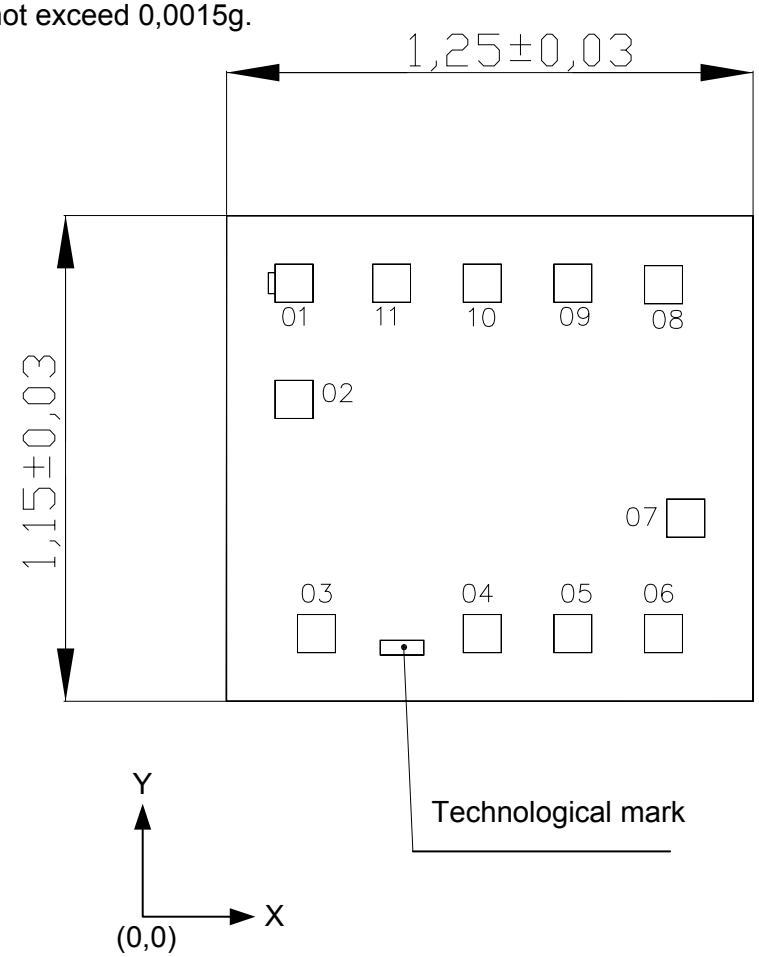


Fig. 9 – Data reading from address Fh

IZ1325 is delivered in the die form
Die weight is not exceed 0,0015g.



Die thichness 0,46±0,02 mm.
Technological mark “1325” coordinates, mm: x = 0,364, y = 0,109.

Fig. 9 – Chip and contact pad layout diagram

Table 7 – Contact pad size and coordinates

Contact pad number	Coordinates (left bottom corner), mm	
	X	Y
01	0,099	0,945
02	0,115	0,670
03	0,168	0,115
04	0,562	0,115
05	0,777	0,115
06	0,992	0,115
07	1,045	0,389
08	0,992	0,942
09	0,777	0,945
10	0,562	0,945
11	0,347	0,945
Note - Contact pad coordinates and dimensions 0,09 x 0,09 mmare indicated under “Passivation” layer		