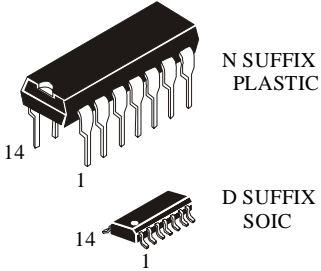


**IW4013B**

**Dual D Flip-Flop**

The IW4013B consists of two identical, independent data-type flip-flops. Each flip-flop has independent data, set, reset, and clock inputs and Q and  $\bar{Q}$  outputs. These devices can be used for shift register applications, and, by connecting  $\bar{Q}$  output to the data input, for counter and toggle applications. The logic level present at the D input is transferred to the Q output during the positive-going transition of the clock pulse. Setting or resetting is independent of the clock and is accomplished by a high level on the set or reset line, respectively.

- Operating Voltage Range: 3.0 to 18 V
- Maximum input current of 1  $\mu$ A at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (over full package temperature range):
  - 1.0 V min @ 5.0 V supply
  - 2.0 V min @ 10.0 V supply
  - 2.5 V min @ 15.0 V supply

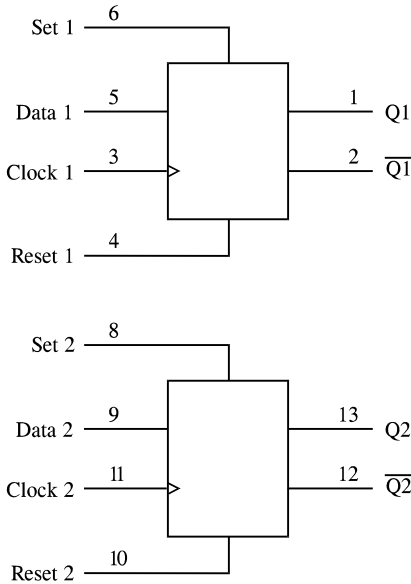


**ORDERING INFORMATION**

IW4013BN Plastic  
 IW4013BD SOIC  
 IZ4013B Chip

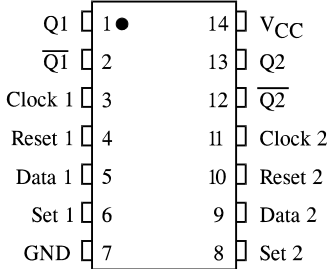
$T_A = -55^\circ$  to  $125^\circ$  C for all packages

**LOGIC DIAGRAM**



PIN 14 =  $V_{CC}$   
 PIN 7 = GND

**PIN ASSIGNMENT**



**FUNCTION TABLE**

Inputs				Outputs	
Clock	Data	Reset	Set	Q	$\bar{Q}$
	L	L	L	L	H
	H	L	L	H	L
	X	L	L	Q	$\bar{Q}$
X	X	H	L	L	H
X	X	L	H	H	L
X	X	H	H	H	H

X = don't care

**MAXIMUM RATINGS\***

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	-0.5 to +20	V
V <sub>IN</sub>	DC Input Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
I <sub>IN</sub>	DC Input Current, per Pin	±10	mA
P <sub>D</sub>	Power Dissipation in Still Air, Plastic DIP, SOIC Package	500**	mW
P <sub>tot</sub>	Power Dissipation per Output Transistor	100	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

\*\*Derating: - Plastic DIP from -55 to +100°C  
 - SOIC Package from -55 to +65°C  
 - Plastic DIP: - 12 mW/°C from +100 to +125°C  
 - SOIC Package: : - 7 mW/°C from +65 to +125°C

**RECOMMENDED OPERATING CONDITIONS**

Symbol	Parameter	Min	Max	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	3.0	18	V
V <sub>IN</sub>	DC Input Voltage (Referenced to GND)	0	V <sub>CC</sub>	V
T <sub>A</sub>	Operating Temperature, All Package Types	-55	+125	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation V<sub>IN</sub> should be constrained to the range GND ≤ V<sub>IN</sub> ≤ V<sub>CC</sub>.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

**DC ELECTRICAL CHARACTERISTICS**(Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit			
				≥-55°C	25°C	≤125°C				
V <sub>IH</sub>	Minimum High-Level Input Voltage	V <sub>OUT</sub> =0.5 V or V <sub>CC</sub> - 0.5 V	5.0	3.5	3.5	3.5	V			
		V <sub>OUT</sub> =1.0 V or V <sub>CC</sub> - 1.0 V	10	7	7	7				
		V <sub>OUT</sub> =1.5 V or V <sub>CC</sub> - 1.5 V	15	11	11	11				
V <sub>IL</sub>	Maximum Low - Level Input Voltage	V <sub>OUT</sub> =0.5 V or V <sub>CC</sub> - 0.5 V	5.0	1.5	1.5	1.5	V			
		V <sub>OUT</sub> =1.0 V or V <sub>CC</sub> - 1.0 V	10	3	3	3				
		V <sub>OUT</sub> =1.5 V or V <sub>CC</sub> - 1.5 V	15	4	4	4				
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>IN</sub> =GND or V <sub>CC</sub>	5.0	4.95	4.95	4.95	V			
			10	9.95	9.95	9.95				
			15	14.95	14.95	14.95				
		V <sub>IL</sub> =1.5V, V <sub>IH</sub> =3.5V, I <sub>O</sub> =-1μA	5.0	4.5	4.5	4.5				
		V <sub>IL</sub> =3.0V, V <sub>IH</sub> =7.0V, I <sub>O</sub> =-1μA	10	9.0	9.0	9.0				
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>IN</sub> =GND or V <sub>CC</sub>	5.0	0.05	0.05	0.05	V			
			10	0.05	0.05	0.05				
			15	0.05	0.05	0.05				
		V <sub>IL</sub> =1.5V, V <sub>IH</sub> =3.5V, I <sub>O</sub> =1μA	5.0	0.5	0.5	0.5				
		V <sub>IL</sub> =3.0V, V <sub>IH</sub> =7.0V, I <sub>O</sub> =1μA	10	1.0	1.0	1.0				
I <sub>IN</sub>	Maximum Input Leakage Current	V <sub>IN</sub> = GND or V <sub>CC</sub>	18	±0.1	±0.1	±1.0	μA			
		I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>IN</sub> = GND or V <sub>CC</sub>	5.0	1		1	30	μA
				10	2	2		60		
15	4			4	120					
20	20			20	600					
I <sub>OL</sub>	Minimum Output Low (Sink) Current	V <sub>IN</sub> = GND or V <sub>CC</sub>					mA			
		U <sub>OL</sub> =0.4 V	5.0	0.64	0.51	0.36				
		U <sub>OL</sub> =0.5 V	10	1.6	1.3	0.9				
		U <sub>OL</sub> =1.5 V	15	4.2	3.4	2.4				
I <sub>OH</sub>	Minimum Output High (Source) Current	V <sub>IN</sub> = GND or V <sub>CC</sub>					mA			
		U <sub>OH</sub> =2.5 V	5.0	-2.0	-1.6	-1.15				
		U <sub>OH</sub> =4.6 V	5.0	-0.64	-0.51	-0.36				
		U <sub>OH</sub> =9.5 V	10	-1.6	-1.3	-0.9				
		15	-4.2	-3.4	-2.4					

**AC ELECTRICAL CHARACTERISTICS**( $C_L=50\text{pF}$ ,  $R_L=200\text{ k}\Omega$ , Input  $t_r=t_f=20\text{ ns}$ )

Symbol	Parameter	$V_{CC}$ V	Guaranteed Limit			Unit
			$\geq -55^\circ\text{C}$	$25^\circ\text{C}$	$\leq 125^\circ\text{C}$	
$f_{\max}$	Maximum Clock Frequency (Figure 1)	5.0	3.5	3.5	3.0	MHz
		10	8	8	6	
		15	12	12	10	
$t_{PLH}$ , $t_{PHL}$	Maximum Propagation Delay, Clock to Q or $\bar{Q}$ (Figure 1)	5.0	300	300	450	ns
		10	130	130	200	
		15	90	90	150	
$t_{PLH}$	Maximum Propagation Delay, Set to Q or Reset to Q (Figure 2)	5.0	300	300	450	ns
		10	130	130	200	
		15	90	90	150	
$t_{PHL}$	Maximum Propagation Delay, Set to $\bar{Q}$ or Reset to Q (Figure 2)	5.0	400	400	600	ns
		10	170	170	250	
		15	120	120	150	
$t_{TLH}$ , $t_{THL}$	Maximum Output Transition Time, Any Output (Figure 1)	5.0	200	200	250	ns
		10	100	100	150	
		15	80	80	100	
$C_{IN}$	Maximum Input Capacitance	5.0		7.5		pF

**TIMING REQUIREMENTS**( $C_L=50\text{pF}$ ,  $R_L=200\text{ k}\Omega$ , Input  $t_r=t_f=20\text{ ns}$ )

Symbol	Parameter	$V_{CC}$ V	Guaranteed Limit			Unit
			$\geq -55^\circ\text{C}$	$25^\circ\text{C}$	$\leq 125^\circ\text{C}$	
$t_w$	Minimum Pulse Width, Clock (Figure 1)	5.0	140	140	200	ns
		10	60	60	80	
		15	40	40	50	
$t_w$	Minimum Pulse Width, Set or Reset (Figure 2)	5.0	180	180	250	ns
		10	80	80	120	
		15	50	50	80	
$t_{su}$	Minimum Setup Time, Data to Clock (Figure 3)	5.0	40	40	40	ns
		10	20	20	20	
		15	15	15	15	
$t_h$	Minimum Hold Time, Clock to Data (Figure 3)	5.0	5	5	8	ns
		10	5	5	5	
		15	5	5	5	
$t_r$ , $t_f$	Maximum Input Rise or Fall Time, Clock (Figure 1)	5.0	500	500	500	$\mu\text{s}$
		10	30	30	30	
		15	6	6	6	

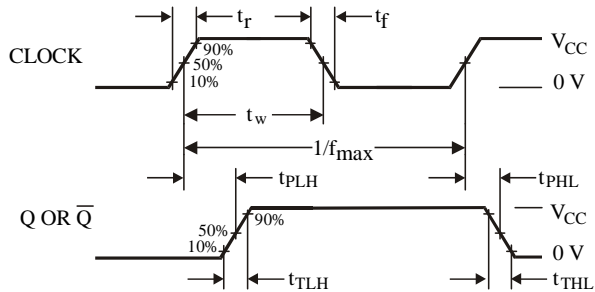


Figure 1. Switching Waveforms

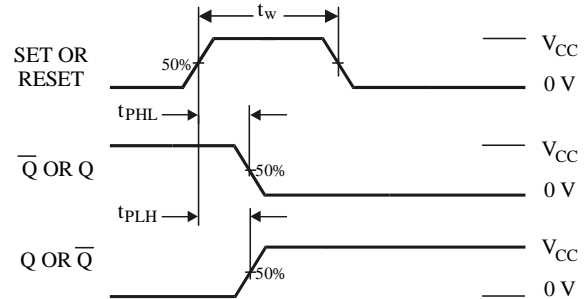


Figure 2. Switching Waveforms

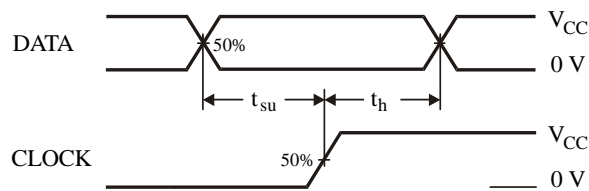
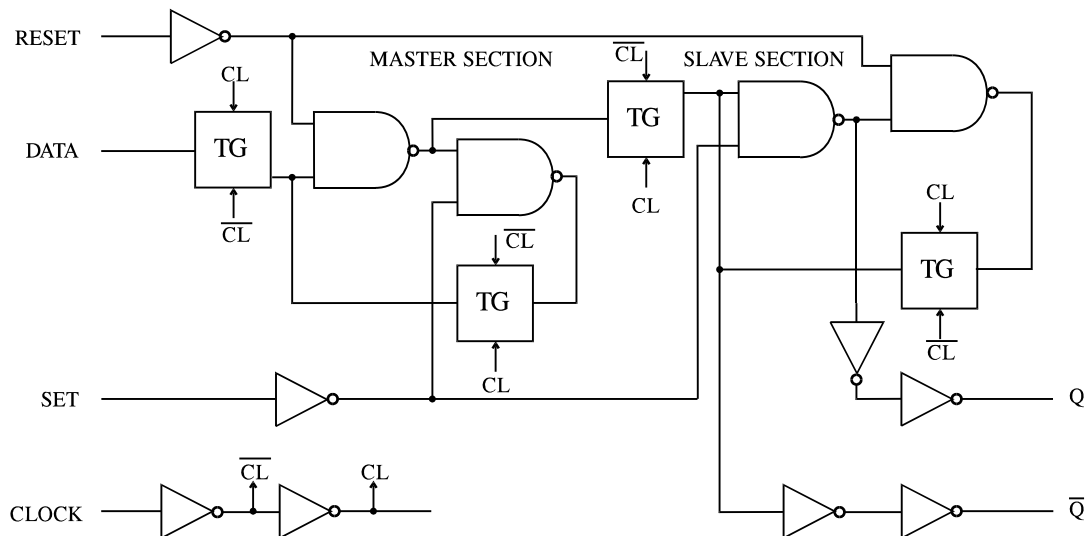
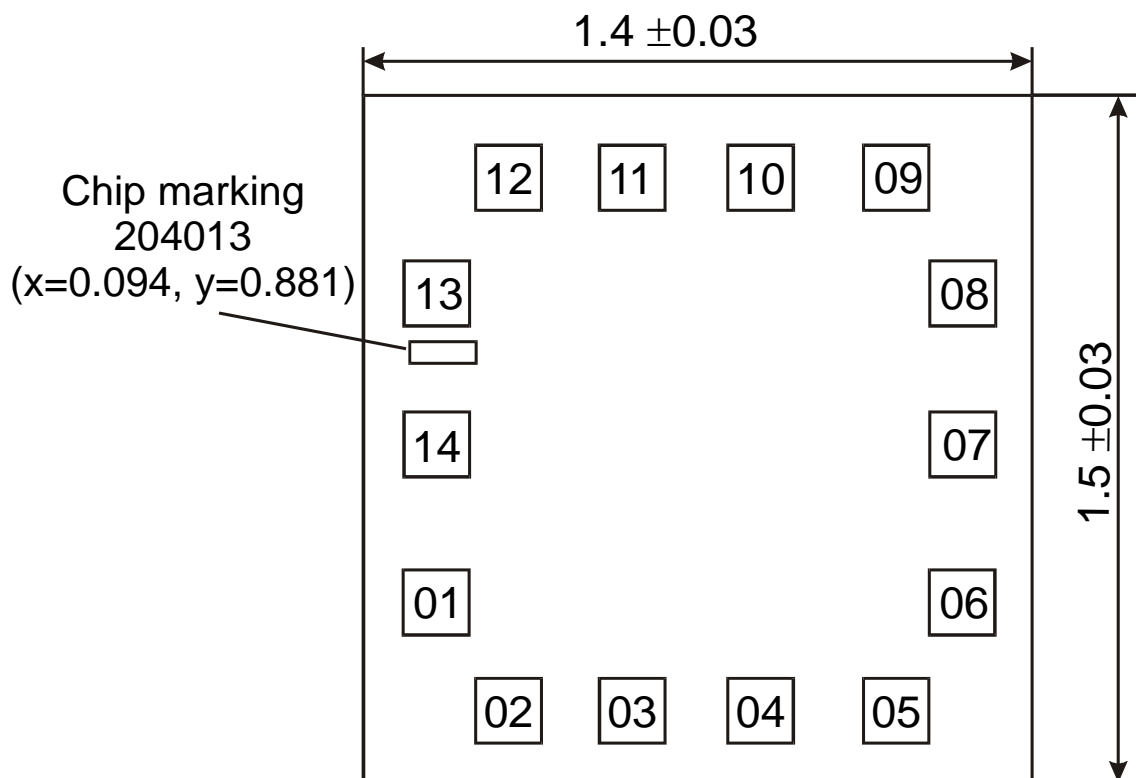


Figure 3. Switching Waveforms

**EXPANDED LOGIC DIAGRAM  
(1/2 of the Device)**



## CHIP PAD DIAGRAM IZ4013B



Pad size 0.100 x 0.100 mm (Pad size is given as per passivation layer)

Thickness of chip  $0.46 \pm 0.02$  mm

## PAD LOCATION

Pad No	Symbol	X	Y
01	$\overline{Q1}$	0.108	0.372
02	$\overline{Q1}$	0.222	0.113
03	Clock 1	0.550	0.113
04	Reset 1	0.833	0.113
05	Data 1	1.074	0.113
06	Set 1	1.191	0.338
07	GND	1.191	0.700
08	Set 2	1.191	1.062
09	Data 2	1.074	1.287
10	Reset 2	0.833	1.287
11	Clock 2	0.550	1.287
12	$\overline{Q2}$	0.222	1.287
13	Q2	0.108	1.028
14	Vcc	0.108	0.698