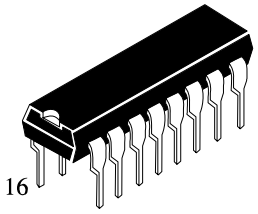
Quad 2-Input Exclusive OR Gate

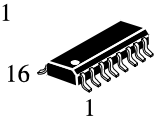
IN74LV86

The 74LV86 is a low–voltage Si–gate CMOS device and is pin and function compatible with the 74HC/HCT86.
The 74LV86 provides the 2-input EXCLUSIVE-OR function.

- Output voltage levels are compatible with input levels of CMOS, NMOS and TTL IC_S
- Supply voltage range: 1.2 to 5.5 V
- Low input current: 1.0 μA; 0.1 μA at T = 25 °C
- Output current: 6 mA at Vcc = 3.0 V; 12 mA at Vcc = 4.5 V
- High Noise Immunity Characteristic of CMOS Devices



N SUFFIX
PLASTIC

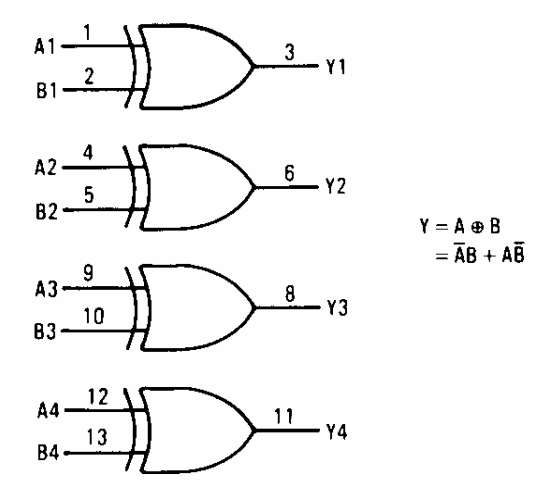


D SUFFIX
SOIC

ORDERING INFORMATION

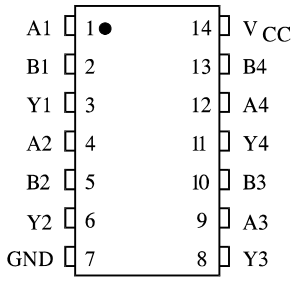
IN74LV86N Plastic
IN74LV86D SOIC
IZ74LV86 Chip
T_A = -40° to 125° C for all packages

LOGIC DIAGRAM



PIN 16=V_{CC}
PIN 08 = GND

PIN ASSIGNMENT



FUNCTION TABLE

Inputs		Outputs
An	Bn	Yn
L	H	H
L	L	L
H	L	H
H	H	L

H= high level
L = low level

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC supply voltage	-0.5 to +5.0	V
I_{IK} *1	Input diode current	±20	mA
I_{OK} *2	Output diode current	±50	mA
I_O *3	Output source or sink current	±25	mA
I_{CC}	V_{CC} current	±50	mA
I_{GND}	GND current	±50	mA
P_D	Power dissipation per package: *4 Plastic DIP SO	 750 500	mW
Tstg	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1.5 mm (Plastic DIP Package), 0.3 mm (SO Package) from Case for 4 Seconds	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.
*1 $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V.
*2 $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V.
*3 -0.5 V $< V_O < V_{CC} + 0.5$ V.
*4 Derating - Plastic DIP: - 12 mW/°C from 70° to 125°C
SO Package: : - 8 mW/°C from 70° to 125°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage		1.2	5.5	V
V_I	DC Input Voltage		0	V_{CC}	V
V_O	DC Output Voltage		0	V_{CC}	V
T_A	Operating Temperature, All Package Types		-40	+125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	1.0 B ≤V_{CC} <2.0 B 2.0 B ≤V_{CC} <2.7 B 2.7 B ≤V_{CC} <3.6 B 3.6 B ≤V_{CC} ≤5.5 B	0 0 0 0	500 200 100 50	ns/V

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range GND≤(V_{IN} or V_{OUT})≤V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test conditions	V_{CC} V	Guaranteed Limit						Unit
				-40°C to 25°C		85°C		125°C		
				min	max	min	max	min	max	
V_{IH}	HIGH level input voltage		1.2 2.0 2.7 3.0 3.6 4.5 5.5	0.9 1.4 2.0 2.0 2.0 3.15 3.85	- - - - - - -	0.9 1.4 2.0 2.0 2.0 3.15 3.85	- - - - - - -	0.9 1.4 2.0 2.0 2.0 3.15 3.85	- - - - - - -	V
V_{IL}	LOW level input voltage		1.2 2.0 2.7 3.0 3.6 4.5 5.5	- - - - - - -	0.3 0.6 0.8 0.8 0.8 1.35 1.65	- - - - - - -	0.3 0.6 0.8 0.8 0.8 1.35 1.65	- - - - - - -	0.3 0.6 0.8 0.8 0.8 1.35 1.65	V
V_{OH}	HIGH level output voltage	$V_I = V_{IH}$ or V_{IL} I_O = -100 μA	1.2 2.0 2.7 3.0 3.6 4.5 5.5	1.05 1.85 2.55 2.85 3.45 4.35 5.35	- - - - - - -	1.0 1.8 2.5 2.8 3.4 4.3 5.3	- - - - - - -	1.0 1.8 2.5 2.8 3.4 4.3 5.3	- - - - - - -	V
		$V_I = V_{IH}$ or V_{IL} I_O = -6 mA	3.0	2.48	-	2.34	-	2.20	-	V
		$V_I = V_{IH}$ or V_{IL} I_O = -12 mA	4.5	3.70	-	3.60	-	3.50	-	V
V_{OL}	LOW level output voltage	$V_I = V_{IH}$ or V_{IL} I_O = 100 μA	1.2 2.0 2.7 3.0 3.6 4.5 5.5	- - - - - - -	0.15 0.15 0.15 0.15 0.15 0.15 0.15	- - - - - - -	0.2 0.2 0.2 0.2 0.2 0.2 0.2	- - - - - - -	0.2 0.2 0.2 0.2 0.2 0.2 0.2	V
		$V_I = V_{IH}$ or V_{IL} I_O = 6 mA	3.0	-	0.33	-	0.40	-	0.50	V
		$V_I = V_{IH}$ or V_{IL} I_O = 12 mA	4.5	-	0.40	-	0.55	-	0.65	V
I_I	Input current	$V_I = V_{CC}$ or 0 V	5.5	-	±0.1	-	±1.0	-	±1.0	μA
I_{CC}	Supply current	$V_I = V_{CC}$ or 0 V I_O = 0 μA	5.5	-	4.0	-	20	-	40	μA
I_{CC1}	Additional quiescent supply current per input	$V_I = V_{CC}$ – 0.6 V	2.7 3.6	-	0.2 0.2	-	0.5 0.5	-	0.85 0.85	mA

AC ELECTRICAL CHARACTERISTICS (C_L=50 pF, R_L = 1 kΩ, t_r=t_f=2.5 ns)

Symbol	Parameter	Test conditions	V_{CC} V	Guaranteed Limit						Unit
				-40°C to 25°C		85°C		125°C		
				min	max	min	max	min	max	
t_{PHL}, t_{PLH}	Propagation delay , An ,Bn, to Yn	V_I = 0 V or V_{CC} Figure 1, 2	1.2 2.0 2.7 3.0 4.5	- - - - -	140 24 19 15 13	- - - - -	150 32 24 19 16	- - - - -	180 41 30 24 20	ns
C_I	Input capacitance	T_A = 25°C	5.0	-	7.0	-	-	-	-	pF
C_{PD}	Power dissipation capacitance (per gate)	V_I = 0 V or V_{CC} T_A = 25°C	5.5	-	60	-	-	-	-	pF

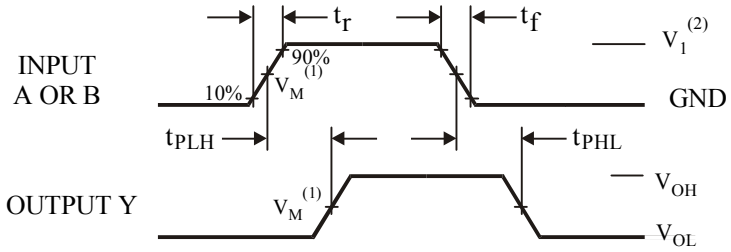
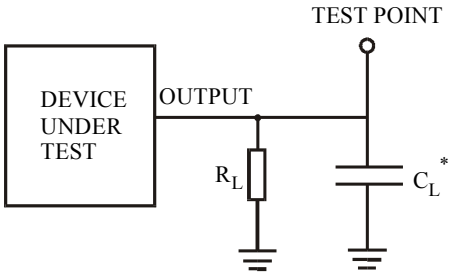


Figure 1. Switching Waveforms

Note:

(1) V_M = 1.5 V at V_{CC} = 2.7 V
V_M = 0.5 ·V_{CC} at V_{CC} =1.2 V, 2.0 V, 3.0 V, 4.5 V

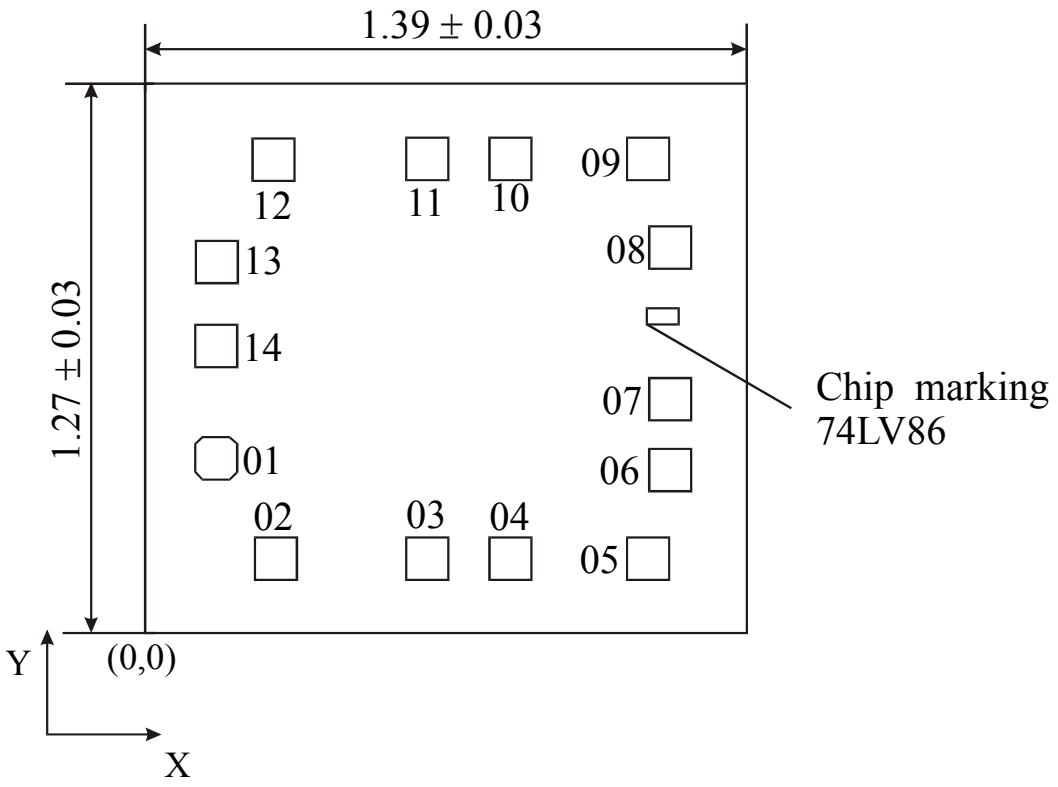
(2) V_I = V_{CC} at V_{CC} =1.2 V, 2.0 V, 2.7 V, 4.5 V
V_I = 2.7 V at V_{CC} = 3.0 V



* Includes all probe and jig capacitance

Figure 4. Test Circuit

CHIP PAD DIAGRAM



Location of marking (mm): left lower corner x=1.159, y=0.7135

Chip thickness: 0.46 ± 0.02 mm.

PAD LOCATION

Pad No	Symbol	Location (left lower corner), mm		Pad size, mm
		X	Y	
01	A1	0.1155	0.3545	0.108 x 0.108
02	B1	0.2505	0.1230	0.108 x 0.108
03	Y1	0.6030	0.1230	0.108 x 0.108
04	A2	0.7955	0.1230	0.108 x 0.108
05	B2	1.1135	0.1230	0.108 x 0.108
06	Y2	1.1650	0.3280	0.108 x 0.108
07	GND	1.1645	0.4915	0.108 x 0.108
08	Y3	1.1650	0.8420	0.108 x 0.108
09	A3	1.1135	1.0470	0.108 x 0.108
10	B3	0.7955	1.0407	0.108 x 0.108
11	Y4	0.6030	1.0407	0.108 x 0.108
12	A4	0.2505	1.0407	0.108 x 0.108
13	B4	0.1155	0.8080	0.108 x 0.108
14	V_{CC}	0.1210	0.6145	0.108 x 0.108

Note: Pad location is given as per metallization layer