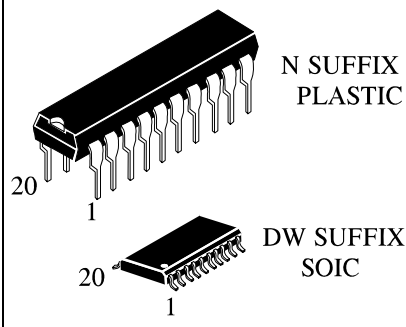**IN74LV373**

Octal D-type transparent latch; 3-state

The IN74LV373 is a low-voltage Si-gate CMOS devise and is pin and function compatible with 74HCT373.

The IN74LV373 is an octal D-type transparent latch featuring separate D-type inputs for each latch and 3-state outputs for bus oriented applications. A latch enable (LE) input and an output enable (OE) input are common to all intemal latches.
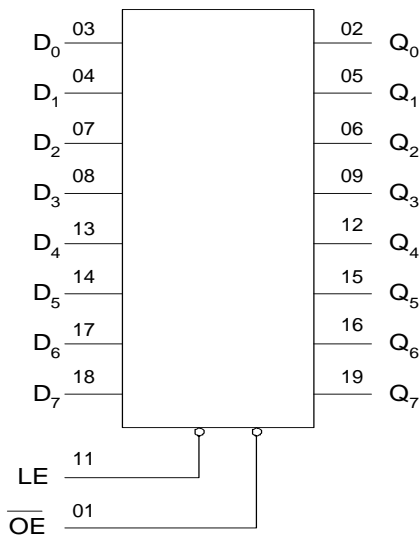
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 1.2 to 3.6 V
- Low Input Current: 1.0 μA
- High Noise Immunity Characteristic of CMOS Devices

N SUFFIX
PLASTIC

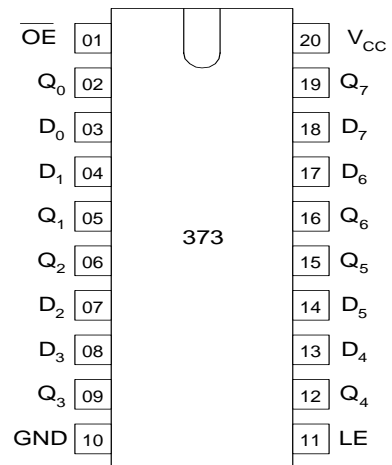DW SUFFIX
SOIC

ORDERING INFORMATION
IN74LV373N   Plastic
IN74LV373DW   SOIC
IZ74LV373   Chip
T_A = -40° to 125° C
for all packages

LOGIC DIAGRAM

D_0 03
D_1 04
D_2 07
D_3 08
D_4 13
D_5 14
D_6 17
D_7 18

02 Q_0
05 Q_1
06 Q_2
09 Q_3
12 Q_4
15 Q_5
16 Q_6
19 Q_7

LE 11
$\overline{OE}$ 01

PIN 20 = V_{CC}
PIN 10 = GND

PIN ASSIGNMENT

$\overline{OE}$	01	20	V_{CC}
Q_0	02	19	Q_7
D_0	03	18	D_7
D_1	04	17	D_6
Q_1	05	16	Q_6
Q_2	06	15	Q_5
D_2	07	14	D_5
D_3	08	13	D_4
Q_3	09	12	Q_4
GND	10	11	LE

373

FUNCTION TABLE

Inputs			Output
$\overline{OE}$	LE	Dn	Qn
L	H	H	H
L	H	L	L
L	L	X	Qo
H	X	X	Z

X = Don't care
Z = High impedance OFF-state
L = Low voltage level
H = HIGH voltage level

INTEGRAL

1

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC supply voltage	-0.5 to +5.0	V
I_{IK}*1	DC input diode current	±20	mA
I_{OK}*2	DC output diode current	±50	mA
I_O*3	DC output source or sink current -bus driver outputs	±35	mA
I_{GND}	DC V_{CC} or GND current for types with - bus driver outputs	±70	mA
I_{CC}	DC V_{CC} or GND current for types with - bus driver outputs	±70	mA
P_D	Power dissipation per paskade, plastic DIP+ SOIC package+	750 500	mW
Tstg	Storage temperature	-65 to +150	°C
T_L	Lead temperature, 1.5 mm from Case for 10 seconds (Plastic DIP), 0.3 mm (SOIC Package)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.
+Derating - Plastic DIP: - 12 mW/°C from 70° to 125°C
          SOIC Package: : - 8 mW/°C from 70° to 125°C
*1: V_I < -0.5 or V_I > V_{CC}+0.5V
*2: Vo < -0.5 or Vo > V_{CC}+0.5V
*3: -0.5V < Vo < V_{CC}+0.5V

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage		1.2	3.6	V
V_{IN}, V_{OUT}	DC Input Voltage, Output Voltage		0	V_{CC}	V
T_A	Operating Temperature, All Package Types		-40	+125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	V_{CC} =1.2 V	0	1000	ns
		V_{CC} =2.0 V	0	700	
		V_{CC} =3.0 V	0	500	
		V_{CC} =3.6 V		400	

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range GND≤(V_{IN} or V_{OUT})≤V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

INTEGRAL

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC}, B	Guaranteed Limit						Unit
				25°C		-40°C to 85°C		-40°C to 125°C		
				min	max	min	max	min	max	
V_{IH}	HIGH level input voltage	$V_O = V_{CC}$-0.1 B	1.2 2.0 3.0 3.6	0.9 1.4 2.1 2.5	- - - -	0.9 1.4 2.1 2.5	- - - -	0.9 1.4 2.1 2.5	- - - -	B
V_{IL}	LOW level input voltage	V_O =0.1 B	1.2 2.0 3.0 3.6	- - - -	0.3 0.6 0.9 1.1	- - - -	0.3 0.6 0.9 1.1	- - - -	0.3 0.6 0.9 1.1	B
V_{OH}	HIGH level output voltage; all outputs	$V_I = V_{IH}$ or V_{IL} I_O = -50 мкА	1.2 2.0 3.0 3.6	1.1 1.92 2.92 3.52	- - - -	1.0 1.9 2.9 3.5	- - - -	1.0 1.9 2.9 3.5	- - - -	B
	HIGH level output voltage; bus driver outputs	$V_I = V_{IH}$ or V_{IL} I_O = -8.0 мА	3.0	2.48	-	2.34	-	2.20	-	B
V_{OL}	LOW-level output voltage; all outputs	$V_I = V_{IH}$ or V_{IL} I_O = 50 мкА	1.2 2.0 3.0 3.6	- - - -	0.09 0.09 0.09 0.09	- - - -	0.1 0.1 0.1 0.1	- - - -	0.1 0.1 0.1 0.1	B
	LOW-level output voltage; bus driver outputs	$V_I = V_{IH}$ or V_{IL} I_O = 8.0 мА	3.0	-	0.33	-	0.4	-	0.5	B
I_{IN}	Input leakage current	$V_I = V_{CC}$ or GND	3.6	-	±0.1	-	±1.0	-	±1.0	мкА
I_{OZ}	3-state output OFF-state current	$V_I = V_{IL}$ or V_{IH} V_O =V_{CC} or GND	1.2 3.6	-	±0.5	-	±5	-	±10	мкА
I_{CC}	Guiescent supply current; MSI	V_I =V_{CC} or 0 B I_O = 0 мкА	3.6	-	8.0	-	80	-	160	мкА

AC ELECTRICAL CHARACTERISTICS $(C_L=50 \text{ пФ}, t_{LH} = t_{HL} = 6.0 \text{ нс}, V_{IL}=0B, V_{IH}=V_{CC})$

Symbol	Parameter	V_{CC} V	Guaranteed Limit						Unit
			25°C		-40°C to 85°C		-40°C to 125°C		
			min	max	min	max	min	max	
t_{PHL}, t_{PLH} от Dn к Qn	Propagation delay Dn to Qn	1.2 2.0 3.0	- - -	150 38 23	- - -	190 48 29	- - -	220 58 35	ns
t_{PHL}, t_{PLH} от LE к Qn	Propagation delay LE to Qn	1.2 2.0 3.0	- - -	180 45 27	- - -	230 56 34	- - -	270 68 41	
t_{PHZ}, t_{PLZ} от OE к Qn	3-state output enable time OE to Qn	1.2 2.0 3.0	- - -	160 35 23	- - -	200 43 28	- - -	240 45 32	
t_{PZH}, t_{PZL} от OE к Qn	3-state output disable time OE to Qn	1.2 2.0 3.0	- - -	160 40 24	- - -	200 50 30	- - -	240 60 36	
t_{THL}, t_{TLH}	Output transition time	1.2 2.0 3.0	- - -	75 16 10	- - -	100 20 13	- - -	120 24 15	
t_W	LE pulse width HING	1.2 2.0 3.0	250 30 18	- - -	350 34 24	- - -	450 41 24	- - -	
t_{SU}	Hold time Dn to LE	1.2 2.0 3.0	45 15 9	- - -	50 17 10	- - -	100 15 12	- - -	
t_H	Hold time Dn to LE	1.2 2.0 3.0	25 5 5	- - -	25 5 5	- - -	25 5 5	- - -	
C_I	Input capacitance	3.0	-	7.0	-	7.0	-	7.0	pF

C_{PD}	Power dissipation capacitance per latch	Typical @25°C, $V_{CC}=3.0$ V	pF
		80	

Used to determine the no-load dynamic power consumption: $P_D = C_{PD}V_{CC}^2 f_i + \sum(C_L V_{CC}^2 f_0)$ where:
f_i = input freguercy in MHz; C_L = output load capacity in pF;
f_0 = output freguercy in MHz; V_{CC} = supply voltage in V;
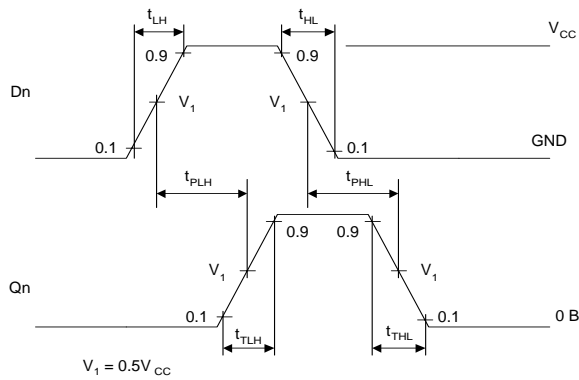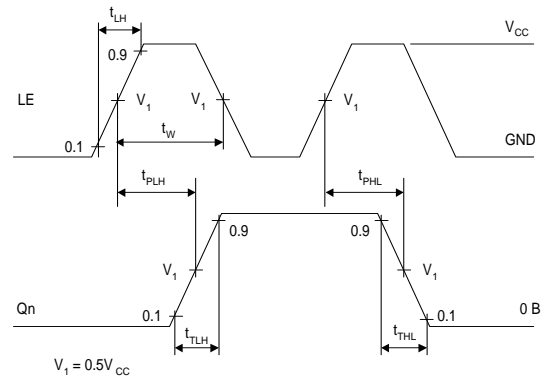$\sum(C_L V_{CC}^2 f_0)$ = sum of outputs.

Figure 1. Switching Waveforms

Figure 2. Switching Waveforms

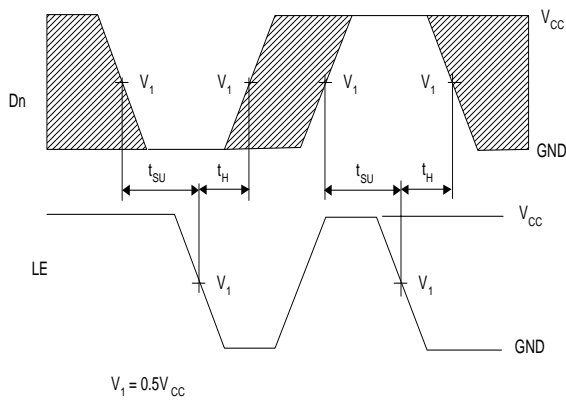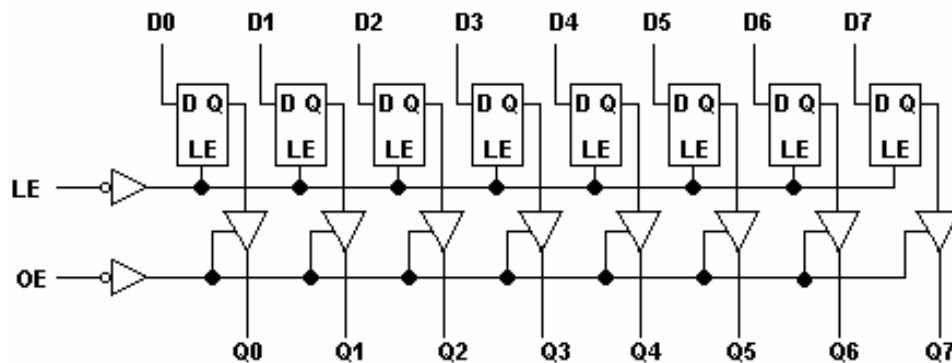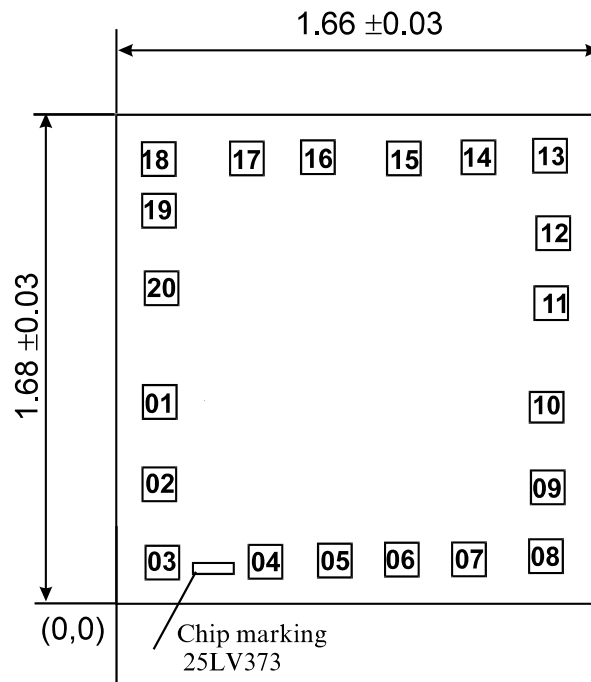**Figure 3. Switching Waveforms**

Figure 4. Switching Waveforms

EXPANDED LOGIC DIAGRAM

CHIP PAD DIAGRAM

1.66 ±0.03

1.68 ±0.03

(0,0)

Chip marking
25LV373

Location of marking (mm): left lower corner x = 0.110, y = 0.306;
Thickness of chip: 0.46 ± 0.02 mm

PAD LOCATION

Pad No	Symbol	Lokation (left lower corner) mm		Pad size (mm)
		X	**Y**	
01	$\overline{OE}$	0.142	0.628	0.108 x 0.108
02	Q0	0.142	0.377	0.108 x 0.108
03	D0	0.142	0.125	0.108 x 0.108
04	D1	0.125	0.125	0.108 x 0.108
05	Q1	0.125	0.125	0.108 x 0.108
06	Q2	0.125	0.125	0.108 x 0.108
07	D2	0.125	0.125	0.108 x 0.108
08	D3	1.423	0.130	0.108 x 0.108
09	Q3	1.423	0.329	0.108 x 0.108
10	GND	1.423	0.587	0.108 x 0.108
11	LE	1.423	0.949	0.108 x 0.108
12	Q4	1.423	1.198	0.108 x 0.108
13	D4	1.423	1.447	0.108 x 0.108
14	D5	1.085	1.447	0.108 x 0.108
15	Q5	0.868	1.447	0.108 x 0.108
16	Q6	0.696	1.447	0.108 x 0.108
17	D6	0.461	1.447	0.108 x 0.108
18	D7	0.142	1.447	0.108 x 0.108
19	Q7	0.142	1.245	0.108 x 0.108
20	Vcc	0.142	0.997	0.108 x 0.108

∗ Note: Pad location is given as per metallization layer

INTEGRAL