

**IN74LV273**

**Octal D Flip-Flop with Common Clock and Reset**

The IN74LV273 is a low-voltage Si-gate CMOS device and is pin and function compatible with the 74HC/HCT273.

The IN74LV273 has eight edge-triggered, D-type flip-flops with individual D inputs and Q outputs. The common clock (CP) and master reset (MR) inputs load and reset (clear) all flip-flops simultaneously. The state of each D input, one set-up time before the LOW-to-HIGH clock transition, is transferred to the corresponding output (Qn) of the flip-flop. All outputs will be forced LOW independently of clock or data inputs by a LOW voltage level on the MR input. The device is useful for applications where the true output only is required and the clock and master reset are common to all storage elements.

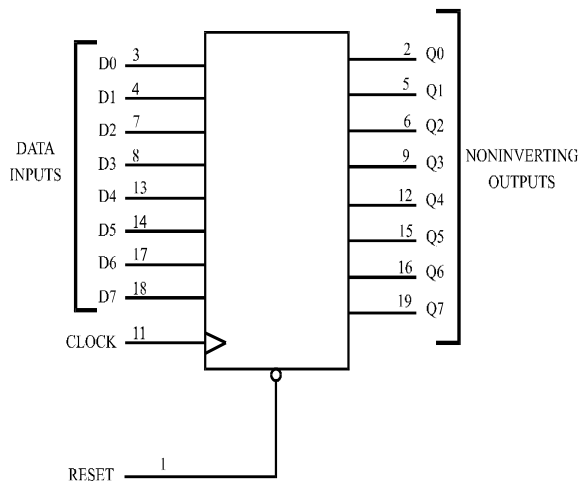
- Output voltage levels are compatible with input levels of CMOS, NMOS and TTL ICs
- Supply voltage range: 1.2 to 5.5 V
- Low input current: 1.0  $\mu$ A; 0.1  $\mu$ A at T = 25 °C
- High Noise Immunity Characteristic of CMOS Devices

**ORDERING INFORMATION**

<b>IN74LV273N</b>	Plastic DIP
<b>IN74LV273DW</b>	SOIC
<b>IZ74LV273</b>	chip

T<sub>A</sub> = -40° to 125° C for all packages

**LOGIC DIAGRAM**



PIN 20 = V<sub>CC</sub>  
PIN 10 = GND

**PIN ASSIGNMENT**

RESET	1	20	V <sub>CC</sub>
Q0	2	19	Q7
D0	3	18	D7
D1	4	17	D6
Q1	5	16	Q6
Q2	6	15	Q5
D2	7	14	D5
D3	8	13	D4
Q3	9	12	Q4
GND	10	11	CLOCK

**FUNCTION TABLE**

Inputs			Output
Reset	Clock	D	Q
L	X	X	L
H		H	H
H		L	L
H	L	X	no change
H		X	no change

H= high level  
L = low level  
X = don't care  
Z = high impedance

**MAXIMUM RATINGS\***

Symbol	Parameter	Value	Unit
$V_{CC}$	DC supply voltage	-0.5 to +7.0	V
$I_{IK}^{*1}$	Input diode current	$\pm 20$	mA
$I_{OK}^{*2}$	Output diode current	$\pm 50$	mA
$I_O^{*3}$	Output source or sink current	$\pm 25$	mA
$I_{CC}$	$V_{CC}$ current	$\pm 50$	mA
$I_{GND}$	GND current	$\pm 50$	mA
$P_D$	Power dissipation per package: Plastic DIP <sup>*4</sup> SO <sup>*4</sup>	750 500	mW
Tstg	Storage Temperature	-65 to +150	°C
$T_L$	Lead Temperature, 1.5 mm (Plastic DIP Package), 0.3 mm (SO Package) from Case for 4 Seconds	260	°C

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

\*<sup>1</sup>  $V_I < -0.5\text{ V}$  or  $V_I > V_{CC} + 0.5\text{ V}$ .

\*<sup>2</sup>  $V_O < -0.5\text{ V}$  or  $V_O > V_{CC} + 0.5\text{ V}$ .

\*<sup>3</sup>  $-0.5\text{ V} < V_O < V_{CC} + 0.5\text{ V}$ .

\*<sup>4</sup> Derating - Plastic DIP: - 12 mW/°C from 70° to 125°C  
SO Package: - 8 mW/°C from 70° to 125°C

**RECOMMENDED OPERATING CONDITIONS**

Symbol	Parameter	Min	Max	Unit
$V_{CC}$	DC Supply Voltage	1.2	5.5	V
$V_I$	DC Input Voltage	0	$V_{CC}$	V
$V_O$	DC Output Voltage	0	$V_{CC}$	V
$T_A$	Operating Temperature, All Package Types	-40	+125	°C
$t_r, t_f$	Input Rise and Fall Time (Figure 1)			ns
	$0\text{ V} \leq V_{CC} \leq 2.0\text{ V}$	0	500	
	$2.0\text{ V} \leq V_{CC} \leq 2.7\text{ V}$	0	200	
	$2.7\text{ V} \leq V_{CC} \leq 3.6\text{ V}$	0	100	
	$3.6\text{ V} \leq V_{CC} \leq 5.5\text{ V}$	0	50	

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{IN}$  and  $V_{OUT}$  should be constrained to the range  $GND \leq (V_{IN} \text{ or } V_{OUT}) \leq V_{CC}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or  $V_{CC}$ ). Unused outputs must be left open.

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

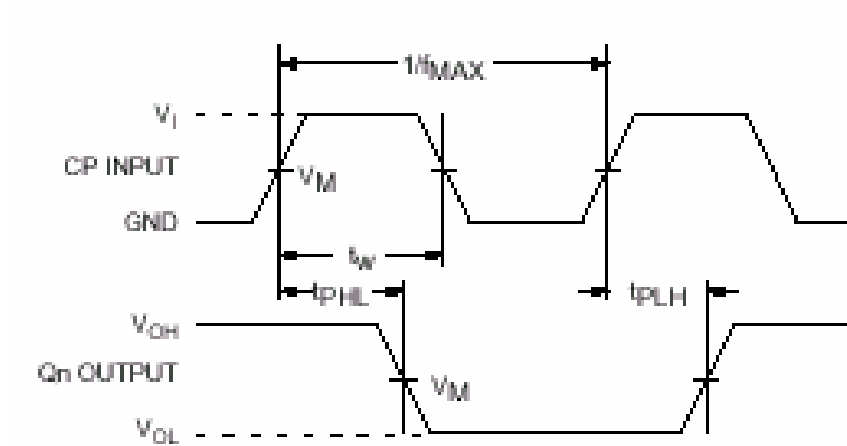
Symbol	Parameter	Test conditions	V <sub>CC</sub> V	Guaranteed Limit								Unit
				25°C		-40°C		85°C		125°C		
				min	max	min	max	min	max	min	max	
V <sub>IH</sub>	HIGH level input voltage		1.2	0.9	-	0.9	-	0.9	-	0.9	-	V
			2.0	1.4	-	1.4	-	1.4	-	1.4	-	
			2.7	2.0	-	2.0	-	2.0	-	2.0	-	
			3.0	2.0	-	2.0	-	2.0	-	2.0	-	
			3.6	2.0	-	2.0	-	2.0	-	2.0	-	
			4.5	3.15	-	3.15	-	3.15	-	3.15	-	
			5.5	3.85	-	3.85	-	3.85	-	3.85	-	
V <sub>IL</sub>	LOW level output voltage		1.2	-	0.3	-	0.3	-	0.3	-	0.3	V
			2.0	-	0.6	-	0.6	-	0.6	-	0.6	
			2.7	-	0.8	-	0.8	-	0.8	-	0.8	
			3.0	-	0.8	-	0.8	-	0.8	-	0.8	
			3.6	-	0.8	-	0.8	-	0.8	-	0.8	
			4.5	-	1.35	-	1.35	-	1.35	-	1.35	
			5.5	-	1.65	-	1.65	-	1.65	-	1.65	
V <sub>OH</sub>	HIGH level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = -100 μA	1.2	1.05	-	1.05	-	1.0	-	1.0	-	V
			2.0	1.85	-	1.85	-	1.8	-	1.8	-	
			2.7	2.55	-	2.55	-	2.5	-	2.5	-	
			3.0	2.85	-	2.85	-	2.8	-	2.8	-	
			3.6	3.45	-	3.45	-	3.4	-	3.4	-	
			4.5	4.35	-	4.35	-	4.3	-	4.3	-	
V <sub>OL</sub>	LOW level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = 100 μA	1.2	-	0.15	-	0.15	-	0.2	-	0.2	V
			2.0	-	0.15	-	0.15	-	0.2	-	0.2	
			2.7	-	0.15	-	0.15	-	0.2	-	0.2	
V <sub>OL</sub>	LOW level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = 6 mA	3.0	-	0.15	-	0.15	-	0.2	-	0.2	V
			3.6	-	0.15	-	0.15	-	0.2	-	0.2	
			4.5	-	0.15	-	0.15	-	0.2	-	0.2	
V <sub>OL</sub>	LOW level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = 12 mA	3.0	-	0.15	-	0.15	-	0.2	-	0.2	V
			3.6	-	0.15	-	0.15	-	0.2	-	0.2	
			4.5	-	0.15	-	0.15	-	0.2	-	0.2	
I <sub>I</sub>	Input current	V <sub>I</sub> = V <sub>CC</sub> or 0 V	5.5	-	±0.1	-	±0.1	-	±1.0	-	±1.0	μA
I <sub>CC</sub>	Supply current	V <sub>I</sub> = V <sub>CC</sub> or 0 V I <sub>O</sub> = 0 μA	5.5	-	8.0	-	8.0	-	80	-	160	μA
I <sub>CC1</sub>	Additional supply current per input	V <sub>I</sub> = V <sub>CC</sub> - 0.6V	2.7 3.6	-	0.2	-	0.2	-	0.5		0.85	mA

AC ELECTRICAL CHARACTERISTICS ( $C_L=50$  pF,  $t_r=t_f=2.5$  ns)

Symbol	Parameter	Test conditions	$V_{CC}$ V	Guaranteed Limit						Unit
				-40°C to 25°C		85°C		125°C		
				min	max	min	max	min	max	
$t_{PHL}, t_{PLH}$	Propagation delay, Clock to Q	$V_1 = 0$ V or $V_1$ Figures 1,4	1.2	-	150	-	150	-	150	ns
			2.0	-	30	-	32	-	41	
			2.7	-	22	-	24	-	30	
			3.0	-	17	-	19	-	24	
			4.5	-	14	-	16	-	20	
$t_{PHL}$	Propagation delay, Reset to Q	$V_1 = 0$ V or $V_1$ Figures 2,4	1.2	-	160	-	160	-	160	ns
			2.0	-	40	-	44	-	56	
			2.7	-	30	-	33	-	41	
			3.0	-	23	-	26	-	33	
			4.5	-	19	-	22	-	28	
$C_I$	Input capacitance		5.0	-	6.0*	-	-	-	-	pF
$C_{PD}$	Power dissipation capacitance (per flip-flop)	$V_1 = 0$ V or $V_{CC}$	5.5	-	40*	-	-	-	-	pF

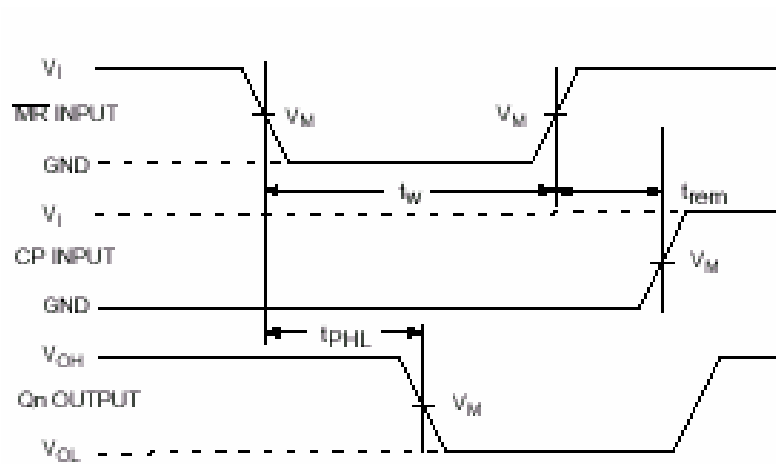
\*  $T = 25^\circ\text{C}$ TIMING REQUIREMENTS ( $C_L=50$  pF,  $t_r=t_f=2.5$  ns)

Symbol	Parameter	Test conditions	$V_{CC}$ V	Guaranteed Limit						Unit
				-40°C to 25°C		85°C		125°C		
				min	max	min	max	min	max	
$t_w$	Pulse Width, Clock (low or high), Reset (low)	$V_1 = 0$ V or $V_1$ Figures 1,2,4	1.2	60	-	70	-	80	-	ns
			2.0	28	-	34	-	41	-	
			2.7	21	-	25	-	30	-	
			3.0	16	-	20	-	24	-	
			4.5	12	-	16	-	20	-	
$t_{su}$	Setup Time, Data to Clock	$V_1 = 0$ V or $V_1$ Figures 3,4	1.2	40	-	50	-	60	-	ns
			2.0	18	-	22	-	26	-	
			2.7	13	-	16	-	19	-	
			3.0	11	-	13	-	15	-	
			4.5	9	-	11	-	13	-	
$t_{rem}$	Removal Time, Reset to Clock	$V_1 = 0$ V or $V_1$ Figures 2,4	1.2	5	-	5	-	5	-	ns
			2.0	5	-	5	-	5	-	
			2.7	5	-	5	-	5	-	
			3.0	5	-	5	-	5	-	
			4.5	5	-	5	-	5	-	
$t_h$	Hold Time, Clock to Data	$V_1 = 0$ V or $V_1$ Figures 3,4	1.2	50	-	50	-	50	-	ns
			2.0	5	-	5	-	5	-	
			2.7	5	-	5	-	5	-	
			3.0	5	-	5	-	5	-	
			4.5	5	-	5	-	5	-	
$f_c$	Clock Frequency	$V_1 = 0$ V or $V_1$ Figures 1,4	1.2	-	2	-	1	-	1	MHz
			2.0	-	17	-	14	-	12	
			2.7	-	23	-	19	-	16	
			3.0	-	30	-	24	-	20	
			4.5	-	32	-	27	-	24	



$V_{OL}$  and  $V_{OH}$  are the typical output voltage drop that occur with the output load.

**Figure 1. Switching Waveforms**



**Figure 2. Switching Waveforms**

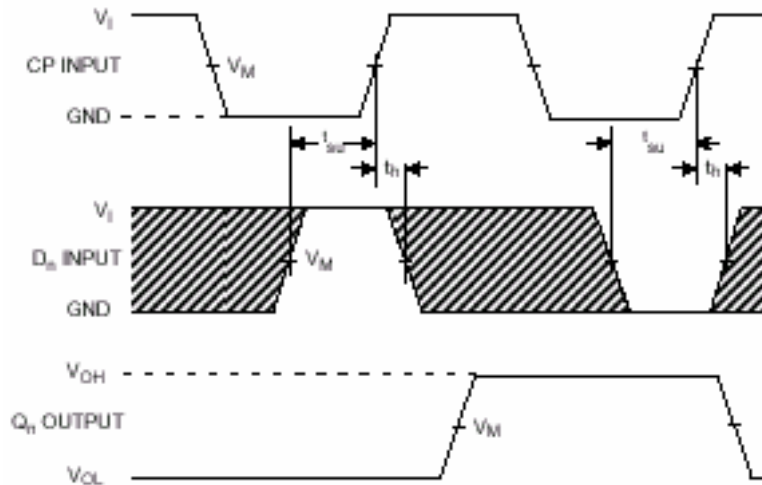
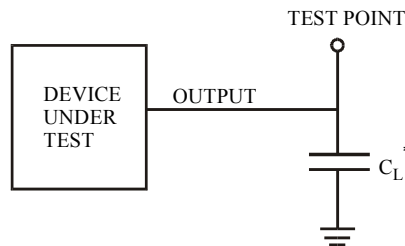


Figure 3. Switching Waveforms

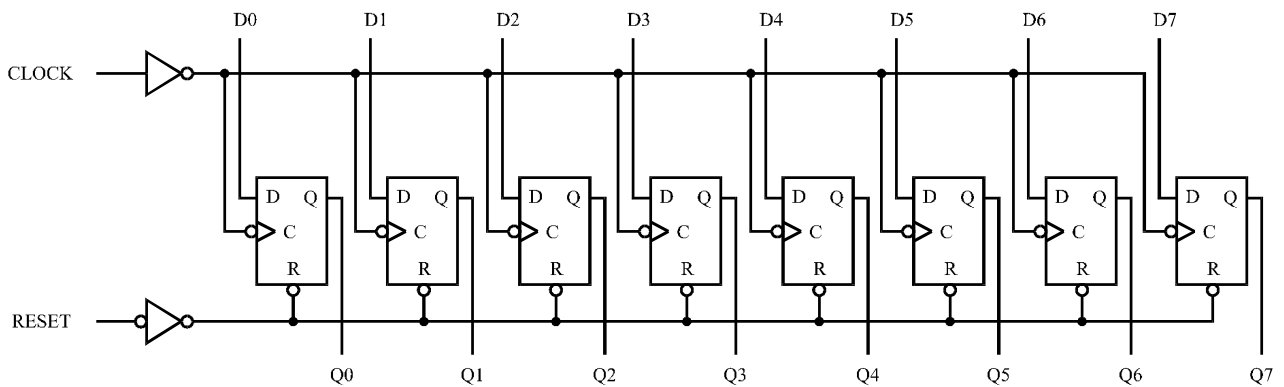
Symbol	Level of a signal, V				
$V_{CC}$	1,2	2,0	2,7	3,0	4,5
$V_I$	1,2	2,0	2,7	2,7	4,5
$V_M$	0,6	1,0	1,5	1,5	2,25



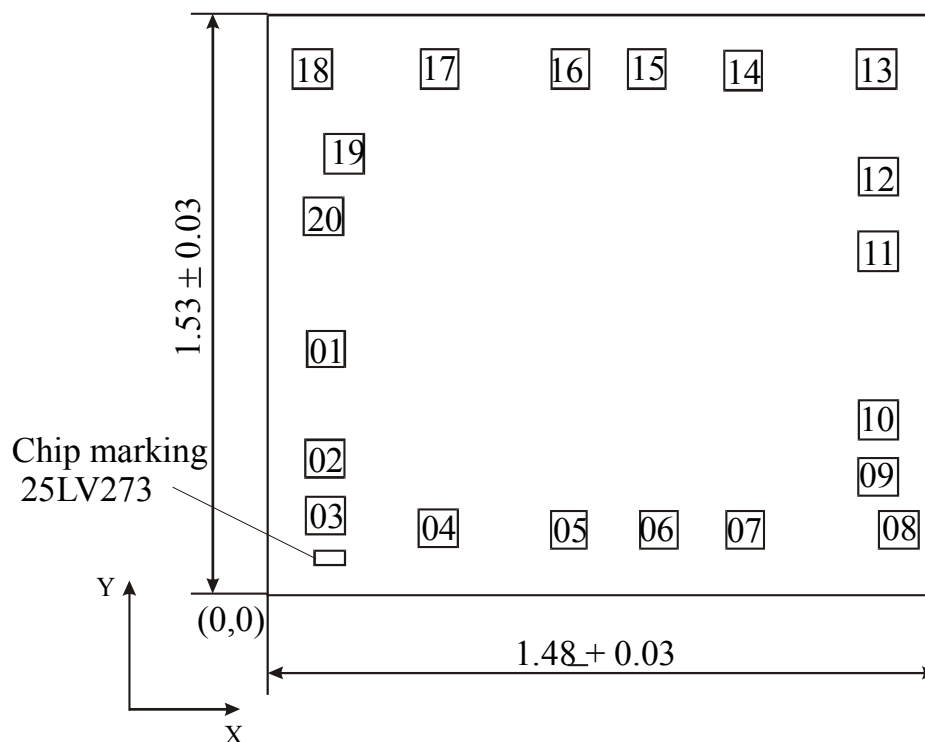
\* Includes all probe and jig capacitance

Figure 4. Test Circuit

**EXPANDED LOGIC DIAGRAM**



## CHIP PAD DIAGRAM



**Location of marking (mm):** left lower corner  $x=0.119$ ,  $y=0.082$ .

**Chip thickness:**  $0.46 \pm 0.02$  mm, ( $0.35 \pm 0.02$  mm – for SOIC).

## PAD LOCATION

Pad No	Symbol	Location (left lower corner), mm		Pad size, mm
		X	Y	
01	Reset	0.1415	0.6270	0.100 x 0.100
02	Q 0	0.1415	0.3880	0.100 x 0.100
03	D 0	0.1375	0.1515	0.100 x 0.100
04	D 1	0.4535	0.1190	0.100 x 0.100
05	Q 1	0.6245	0.1190	0.100 x 0.100
06	Q 2	0.7800	0.1190	0.100 x 0.100
07	D 2	0.9520	0.1180	0.100 x 0.100
08	D 3	1.2685	0.1185	0.100 x 0.100
09	Q 3	1.2480	0.2960	0.100 x 0.100
10	GND	1.2650	0.5160	0.100 x 0.100
11	Clock	1.2650	0.8430	0.100 x 0.100
12	Q 4	1.2425	1.0820	0.100 x 0.100
13	D 4	1.2465	1.3165	0.100 x 0.100
14	D 5	0.9520	1.3120	0.100 x 0.100
15	Q 5	0.7800	1.3110	0.100 x 0.100
16	Q 6	0.6245	1.3110	0.100 x 0.100
17	D 6	0.4535	1.3110	0.100 x 0.100
18	D 7	0.1160	1.3115	0.100 x 0.100
19	Q 7	0.1440	1.1350	0.100 x 0.100
20	V <sub>CC</sub>	0.1190	0.9140	0.100 x 0.100

Note: Pad location is given as per passivation layer.