

IN74LV244

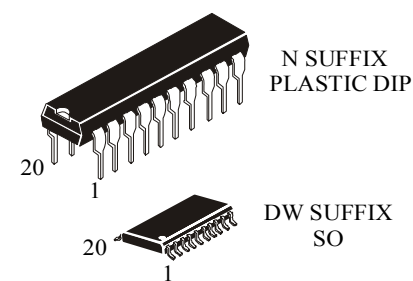
OCTAL BUFFER/LINE DRIVE; 3-STATE

The IN74LV244 is a low-voltage Si-gate CMOS device and is pin and function compatible with IN74HC/HCT244.

The IN74LV244 is an octal non-inverting buffer/line driver with 3-state outputs. The 3-state outputs are controlled by the output enable inputs $\overline{1OE}$ and $\overline{2OE}$. A HIGH on \overline{nOE} causes the outputs to assume a high impedance OFF-state.

The IN74LV244 is identical to the IN74LV240 but has non-inverting outputs.

- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 1.2 to 3.6 V
- Low Input Current: 1.0 μ A, 0.1 μ A at T = 25 °C
- Output Current: 8 mA at $V_{CC} = 3.0$ V
- High Noise Immunity Characteristic of CMOS Devices



N SUFFIX
PLASTIC DIP

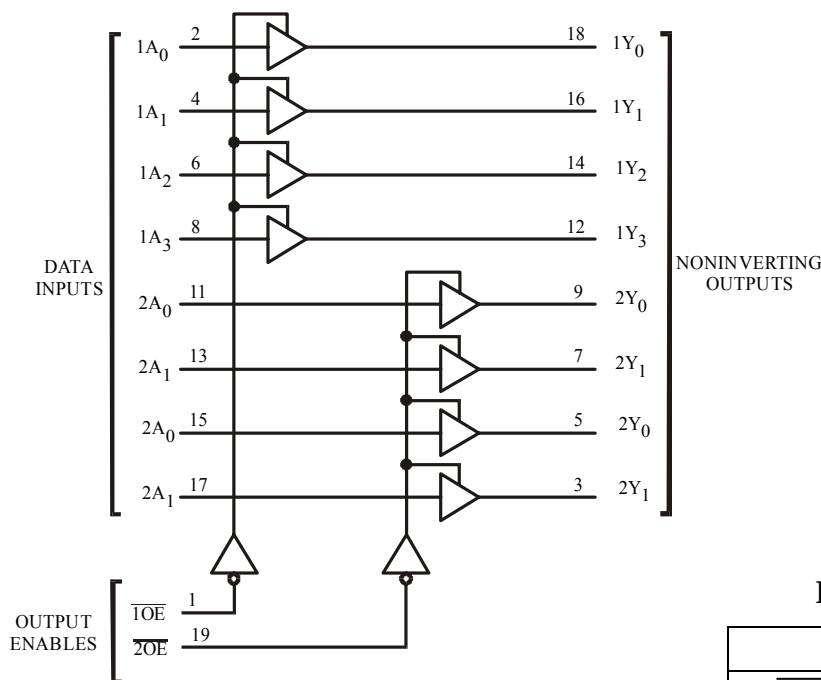
DW SUFFIX
SO

ORDERING INFORMATION

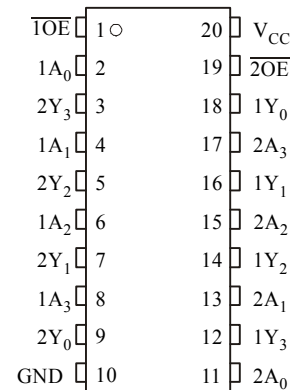
IN74LV244N Plastic DIP
IN74LV244DW SOIC
IZ74LV244 chip

$T_A = -40^\circ$ to 125° C for all packages

LOGIC DIAGRAM



PIN ASSIGNMENT



FUNCTION TABLE

Input		Output
\overline{nOE}	nAn	nYn
L	L	L
L	H	H
H	X	Z

H= high level
 L = low level
 X = don't care
 Z = high impedance

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC supply voltage	-0.5 to +5.0	V
I_{IK}^{*1}	DC Input diode current	± 20	mA
I_{OK}^{*2}	DC Output diode current	± 50	mA
I_O^{*3}	DC Output source or sink current	± 35	mA
I_{CC}	DC V_{CC} current	± 70	mA
I_{GND}	DC GND current	± 70	mA
P_D	Power dissipation per package: * ⁴ Plastic DIP SO	750 500	mW
Tstg	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1.5 mm (Plastic DIP Package), 0.3 mm (SO Package) from Case for 4 Seconds	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

*¹ $V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$.

*² $V_O < -0.5\text{ V}$ or $V_O > V_{CC} + 0.5\text{ V}$.

*³ $-0.5\text{ V} < V_O < V_{CC} + 0.5\text{ V}$.

*⁴ Derating - Plastic DIP: - 12 mW/°C from 70° to 125°C
SO Package: - 8 mW/°C from 70° to 125°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage	1.2	3.6	V
V_I	Input Voltage	0	V_{CC}	V
V_O	Output Voltage	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	-40	+125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)			ns
	$V_{CC} = 1.2\text{ V}$	0	1000	
	$V_{CC} = 2.0\text{ V}$	0	700	
	$V_{CC} = 3.0\text{ V}$	0	500	
	$V_{CC} = 3.6\text{ V}$	0	400	

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range $GND \leq (V_{IN} \text{ or } V_{OUT}) \leq V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test conditions	V _{CC} V	Guaranteed Limit						Unit
				25°C		-40°C to 85°C		125°C		
				min	max	min	max	min	max	
V _{IH}	HIGH level input voltage		1.2	0.9	-	0.9	-	0.9	-	V
			2.0	1.4	-	1.4	-	1.4	-	
			3.0	2.1	-	2.1	-	2.1	-	
			3.6	2.5	-	2.5	-	2.5	-	
V _{IL}	LOW level input voltage		1.2	-	0.3	-	0.3	-	0.3	V
			2.0	-	0.6	-	0.6	-	0.6	
			3.0	-	0.9	-	0.9	-	0.9	
			3.6	-	1.1	-	1.1	-	1.1	
V _{OH}	HIGH level output voltage	V _I = V _{IH} or V _{IL} I _O = -50 μA	1.2	1.1	-	1.0	-	1.0	-	V
			2.0	1.92	-	1.9	-	1.9	-	
			3.0	2.92	-	2.9	-	2.9	-	
			3.6	3.52	-	3.5	-	3.5	-	
		3.0	2.48	-	2.34	-	2.20	-	V	
V _{OL}	LOW level output voltage	V _I = V _{IH} or V _{IL} I _O = 50 μA	1.2	-	0.09	-	0.1	-	0.1	V
			2.0	-	0.09	-	0.1	-	0.1	
			3.0	-	0.09	-	0.1	-	0.1	
			3.6	-	0.09	-	0.1	-	0.1	
		3.0	-	0.33	-	0.4	-	0.5	V	
I _I	Input current	V _I = V _{CC} or 0 V	*	-	±0.1	-	±1.0	-	±1.0	μA
I _{OZ}	Three state leakage current	3-state outputs V _I (01,19) = V _{IH} V _O = V _{CC} or 0 V	1.2 *	-	±0.5	-	±5	-	±10	μA
I _{CC}	Supply current	V _I = V _{CC} or 0 V I _O = 0 μA	*	-	8.0	-	80	-	160	μA

* V_{CC} = 3.3 ± 0.3 V

AC ELECTRICAL CHARACTERISTICS ($C_L=50$ pF, $t_r=t_f=6.0$ ns)

Symbol	Parameter	Test conditions	V _{CC} V	Guaranteed Limit						Unit
				25°C		-40°C to 85°C		125°C		
				min	max	min	max	min	max	
t _{PHL} , t _{PLH}	Propagation delay, 1An to 1Yn, 2An to 2Yn	V _I = 0 V or V _{CC} Figure 1 and 3	1.2 2.0 *	- 100 24 15	- 24 30 19	- 125 30 19	- - - -	- 150 36 23	ns	
t _{PHZ} , t _{PLZ}	Propagation delay, 1OE to 1Yn, 2OE to 2Yn	V _I = 0 V or V _{CC} Figure 2 and 4	1.2 2.0 *	- 140 30 20	- 175 35 24	- - - -	- 210 41 28	ns		
t _{PZH} , t _{PZL}	Propagation delay, 1OE to 1Yn, 2OE to 2Yn	V _I = 0 V or V _{CC} Figure 2 and 4	1.2 2.0 *	- 140 32 20	- 175 40 25	- - - -	- 210 48 30	ns		
t _{THL} , t _{TLH}	Output Transition Time, Any Output	V _I = 0 V or V _{CC} Figure 1 and 3	1.2 2.0 *	- 60 16 10	- 75 20 13	- - - -	- 90 24 15	ns		
C _I	Input capacitance		3.0	- 7.0	- 7.0	- -	- 7.0	pF		
C _{PD}	Power dissipation capacitance (per one channel)	V _I = 0 V or V _{CC}		- 50	- -	- -	- -	pF		

* V_{CC} = 3.3 ± 0.3 V

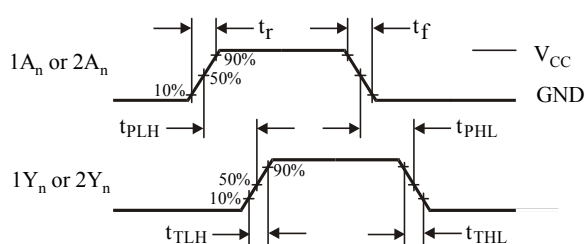


Figure 1. Switching Waveforms

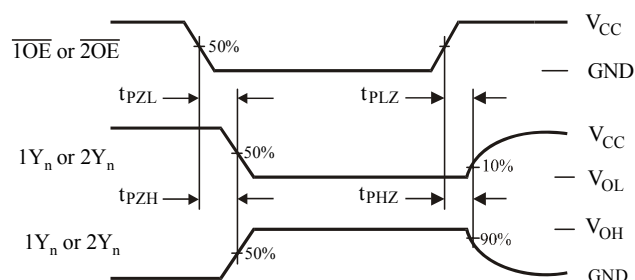
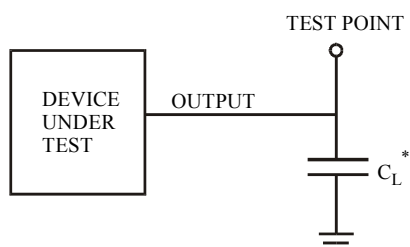
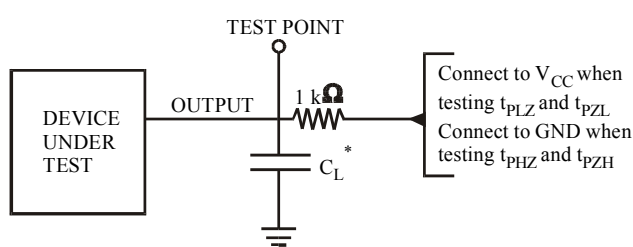


Figure 2. Switching Waveforms



* Includes all probe and jig capacitance

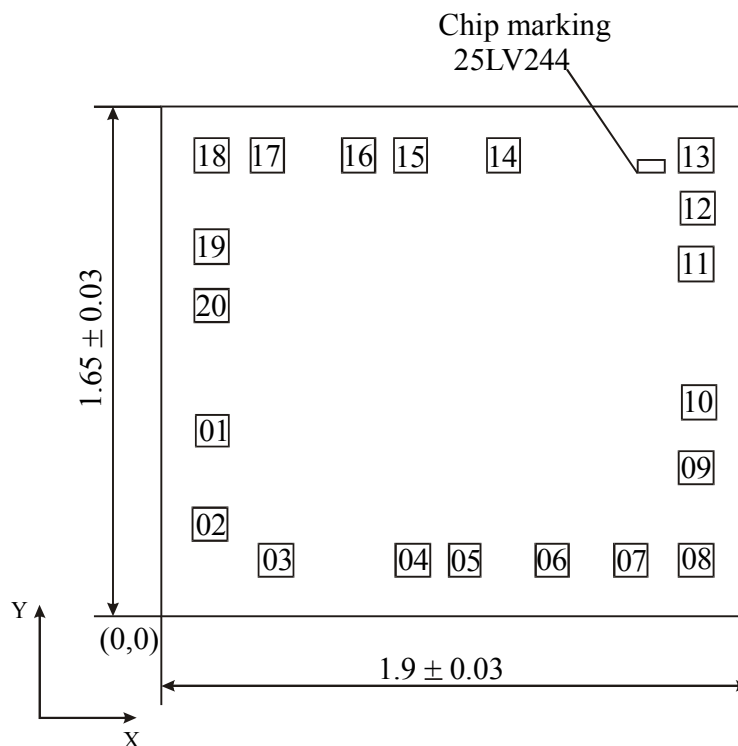
Figure 3. Test Circuit



* Includes all probe and jig capacitance

Figure 4. Test Circuit

CHIP PAD DIAGRAM



Location of marking (mm): left lower corner $x=1.539$, $y=1.433$.

Chip thickness: 0.46 ± 0.02 mm.

PAD LOCATION

Pad No	Symbol	Location (left lower corner), mm		Pad size, mm
		X	Y	
01	$\overline{1OE}$	0.115	0.55	0.108 x 0.108
02	$1A_0$	0.1075	0.246	0.108 x 0.108
03	$2Y_3$	0.3215	0.131	0.108 x 0.108
04	$1A_1$	0.76	0.131	0.108 x 0.108
05	$2Y_2$	0.9285	0.131	0.108 x 0.108
06	$2A_2$	1.2115	0.131	0.108 x 0.108
07	$2Y_1$	1.4615	0.131	0.108 x 0.108
08	$1A_3$	1.674	0.131	0.108 x 0.108
09	$2Y_0$	1.674	0.43	0.108 x 0.108
10	GND	1.685	0.643	0.108 x 0.108
11	$2A_0$	1.674	1.0855	0.108 x 0.108
12	$1Y_3$	1.6795	1.266	0.108 x 0.108
13	$2A_1$	1.674	1.4345	0.108 x 0.108
14	$1Y_2$	1.0525	1.4345	0.108 x 0.108
15	$2A_2$	0.7545	1.4345	0.108 x 0.108
16	$1Y_1$	0.586	1.4345	0.108 x 0.108
17	$2A_3$	0.293	1.4345	0.108 x 0.108
18	$\overline{1Y_0}$	0.112	1.4345	0.108 x 0.108
19	$\overline{2OE}$	0.112	1.1385	0.108 x 0.108
20	V_{CC}	0.112	0.949	0.108 x 0.108

Note: Pad location is given as per metallization layer