

PROGRAMMABLE TIMER

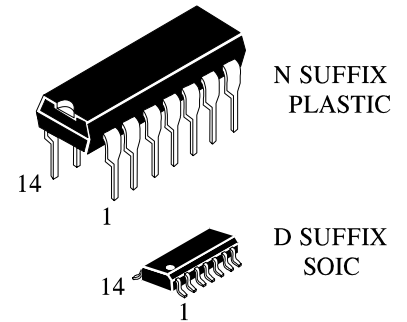
High-Performance Silicon-Gate CMOS

The IW4541 programmable timer consists of a 16-stage binary counter, an oscillator that is controlled by external R-C components (2 resistors and a capacitor), an automatic power-on reset circuit, and output control logic. The counter increments on positive-edge clock transitions and can also be reset via the MASTER RESET input.

The output from this timer is the Q or not Q output from the 8th, 10th, 13th, or 16th counter stage. The desired stage is chosen using time-select inputs A and B. The output is available in either of two modes selectable via the MODE input, pin 10. When this MODE input is a logic "1", the output will be a continuous square wave having a frequency equal to the oscillator frequency divided by 2^N . With the MODE input set to logic "0" and after a MASTER RESET is initiated, the output (assuming Q output has been selected) changes from a low to a high state after 2^{N-1} counts and remains in that state until another MASTER RESET pulse is applied or the MODE input is set to a logic "1".

Timing is initialized by setting the AUTO RESET input (pin 5) to logic "0" and turning power on. If pin 5 is set to logic "1", the AUTO RESET circuit is disabled and counting will not start until after a positive MASTER RESET pulse is applied and returns to a low level. The AUTO RESET consumes an appreciable amount of power and should not be used if low-power operation is desired. For reliable automatic power-on reset, V_{CC} should be greater than 5V.

- Operating Voltage Range: 3.0 to 18 V
- Maximum input current of 1 μ A at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (over full package temperature range):
 1.0 V min @ 5.0 V supply
 2.0 V min @ 10.0 V supply
 2.5 V min @ 15.0 V supply

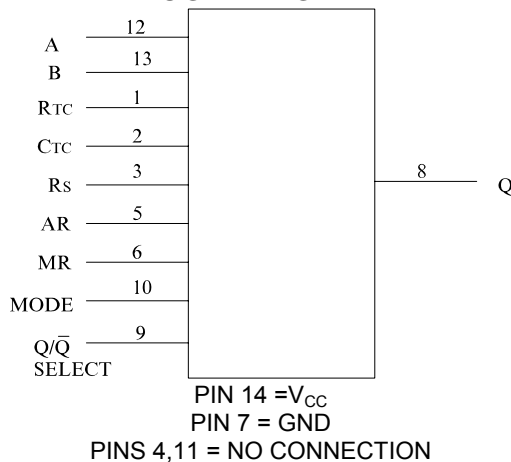


ORDERING INFORMATION

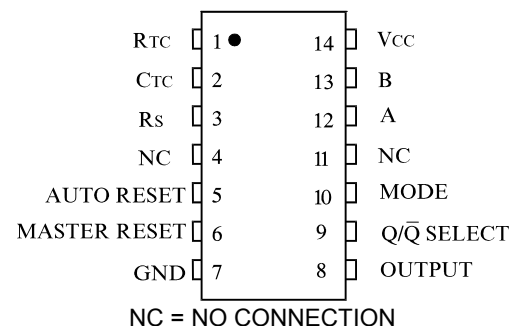
IW4541BN Plastic
 IW4541BD SOIC

$T_A = -55^\circ$ to 125° C for all packages

LOGIC DIAGRAM



PIN ASSIGNMENT



IW4541B

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +20	V
V _{IN}	DC Input Voltage (Referenced to GND)	-0.5 to V _{CC} +0.5	V
V _{OUT}	DC Output Voltage (Referenced to GND)	-0.5 to V _{CC} +0.5	V
I _{IN}	DC Input Current, per Pin	±10	mA
P _D	Power Dissipation in Still Air, Plastic DIP+ SOIC Package+	750 500	mW
P _D	Dissipation per Output Transistor	100	mW
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

+Derating - Plastic DIP: - 10 mW/°C from 65° to 125°C

SOIC Package: : - 7 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	3.0	18	V
V _{IN} , V _{OUT}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V
T _A	Operating Temperature, All Package Types	-55	+125	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range $GND \leq (V_{IN} \text{ or } V_{OUT}) \leq V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

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DC ELECTRICAL CHARACTERISTICS Digital Section

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limit			Unit
				≥ -55 °C	≤ 25 °C	≤ 125 °C	
V _{IH}	Minimum High-Level Input Voltage	V _{OUT} =0.5V or V _{CC} -0.5V V _{OUT} =1.0V or V _{CC} -1.0V V _{OUT} =1.5V or V _{CC} -1.5V	5	3.5	3.5	3.5	V
			10	7	7	7	
			15	11	11	11	
V _{IL}	Maximum Low - Level Input Voltage	V _{OUT} =0.5V or V _{CC} -0.5V V _{OUT} =1.0V or V _{CC} -1.0V V _{OUT} =1.5V or V _{CC} -1.5V	5	1.5	1.5	1.5	V
			10	3	3	3	
			15	4	4	4	
V _{OH}	Minimum High-Level Output Voltage	V _{IN} =GND or V _{CC}	5.0	4.95	4.95	4.95	V
			10	9.95	9.95	9.95	
			15	14.95	14.95	14.95	
V _{OL}	Maximum Low-Level Output Voltage	V _{IN} =GND or V _{CC}	5.0	0.05	0.05	0.05	V
			10	0.05	0.05	0.05	
			15	0.05	0.05	0.05	
I _{IN}	Maximum Input Leakage Current	V _{IN} = GND or V _{CC}	18	±0.1	±0.1	±1.0	μA
I _{CC}	Maximum Quiescent Supply Current (per Package)	V _{IN} = GND or V _{CC}	5.0	5	5	150	μA
			10	10	10	300	
			15	20	20	600	
			20	100	100	3000	
I _{OL}	Minimum Output Low (Sink) Current	V _{IN} = GND or V _{CC} U _{OL} =0.4 V U _{OL} =0.5 V U _{OL} =1.5 V	5.0	1.9	1.55	1.08	mA
			10	5	4	2.8	
			15	12.6	10	7.2	
I _{OH}	Minimum Output High (Source) Current	V _{IN} = GND or V _{CC} U _{OH} =2.5 V U _{OH} =4.6 V U _{OH} =9.5 V U _{OH} =13.5 V	5.0	-6.2	-5	-3	mA
			5.0	-1.9	-1.55	-1.08	
			10	-5	-4	-2.8	
			15	-12.6	-10	-7.2	

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AC ELECTRICAL CHARACTERISTICS ($C_L=50\text{pF}$, $R_L=200\text{k}\Omega$, Input $t_r=t_f=20\text{ ns}$)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			≥ -55 $^{\circ}\text{C}$	25°C	≤ 125 $^{\circ}\text{C}$	
f_{\max}	Maximum Clock Frequency (Figure 1)	5.0	1.5	1.5	0.75	MHz
		10	4	4	2	
		15	6	6	3	
t_{PLH} , t_{PHL}	Maximum Propagation Delay, Clock to Q (Figure 1) (2^8) (2^{16})	5.0	10.5	10.5	21	ns
		10	3.8	3.8	7.6	
		15	2.9	2.9	5.8	
		5.0	18	18	36	
		10	10	10	20	
		15	7.5	7.5	15	
t_{THL}	Maximum Output Transition Time, Any Output (Figure 1)	5.0	200	200	400	ns
		10	100	100	200	
		15	80	80	160	
t_{TLH}	Maximum Output Transition Time, Any Output (Figure 1)	5.0	360	360	720	ns
		10	180	180	360	
		15	130	130	260	
C_{IN}	Maximum Input Capacitance	-		7.5		pF

TIMING REQUIREMENTS ($C_L=50\text{pF}$, $R_L=200\text{k}\Omega$, Input $t_r=t_f=20\text{ ns}$)

Symbol	Parameter	V_{CC}	Guaranteed Limit		Unit
			+25 $^{\circ}\text{C}$	-40 $^{\circ}\text{C}$ to +85 $^{\circ}\text{C}$	
t_w	Minimum Pulse Width, Master Reset or Clock (Figure 1)	5	900	1800	ns
		10	300	600	
		15	225	450	
t_r, t_f	Maximum Rise and Fall Time, Clock (Figure 1)	5	Unlimited		μs
		10			
		15			

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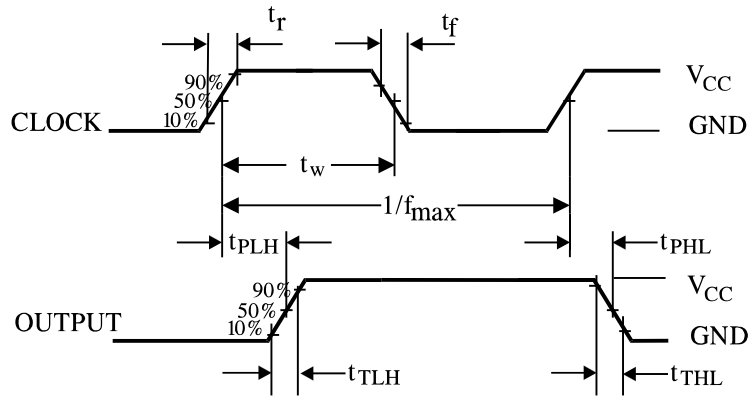


Figure 1. Switching Weveforms

EXPANDED LOGIC DIAGRAM

FREQUENCY SELECTION TABLE

INPUTS		No. of Stages	Count
A	B	N	2^N
L	L	13	8192
L	H	10	1024
H	L	8	256
H	H	16	65536

FUNCTION TABLE

PIN	STATE	
	0	1
5	Auto Reset On	Auto Reset Disable
6	Master Reset Off	Master Reset On
9	Output Initially Low After Reset (Q)	Output Initially High After Reset (not Q)
10	Single Transition Mode	Recycle Mode

