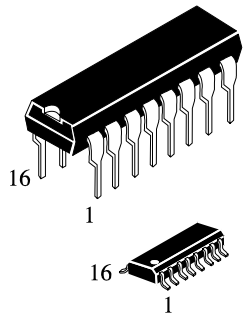
STROBED HEX INVERTER/BUFFER

High-Voltage Silicon-Gate CMOS

The IW4502B consists of six inverter/buffers with 3-state outputs. A logic “1” on the OUTPUT ENABLE input produces a high impedance state in all six outputs. This feature permits common busing of the outputs, thus simplifying system design. A logic “1” on the DIRECTION input switches all six outputs to logic “0” if the OUTPUT ENABLE input is a logic “0”.

- Operating Voltage Range: 3.0 to 18 V
- Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (over full package temperature range):

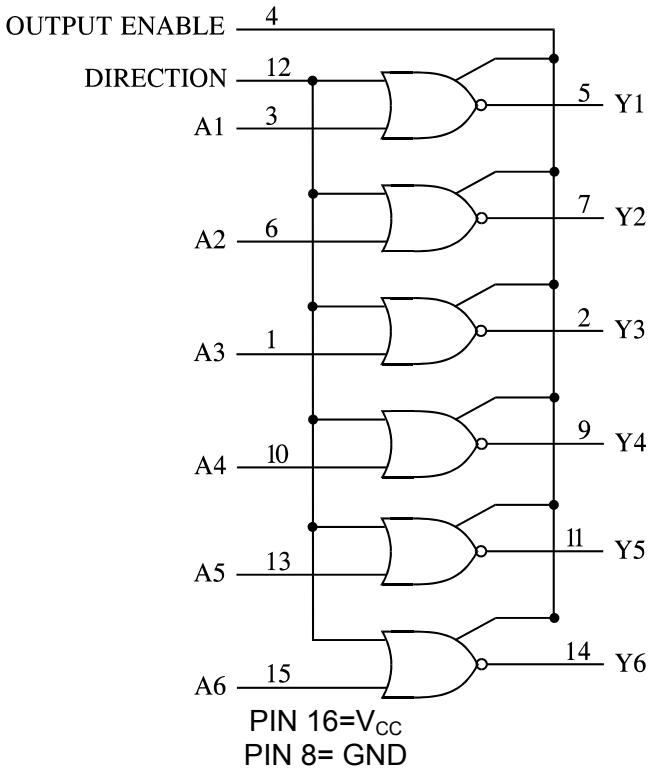
1.0 V min @ 5.0 V supply
2.0 V min @ 10.0 V supply
2.5 V min @ 15.0 V supply



ORDERING INFORMATION

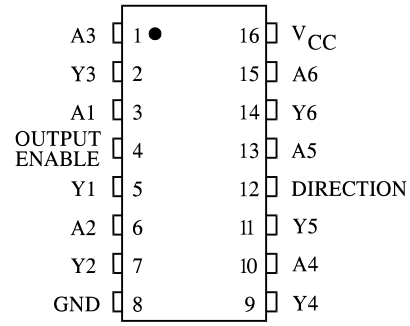
IW4502BN Plastic
IW4502BD SOIC
T_A = -55° to 125° C for all packages

LOGIC DIAGRAM



PIN 16=V_{CC}
PIN 8= GND

PIN ASSIGNMENT



FUNCTION TABLE

Inputs			Output
Output Enable	Direction	A	Y
L	L	L	H
L	L	H	L
L	H	X	L
H	X	X	Z

Z = high impedance
X = don’t care

INTEGRAL

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +20	V
V_{IN}	DC Input Voltage (Referenced to GND)	-0.5 to V_{CC} +0.5	V
V_{OUT}	DC Output Voltage (Referenced to GND)	-0.5 to V_{CC} +0.5	V
I_{IN}	DC Input Current, per Pin	±10	mA
P_D	Power Dissipation in Still Air, Plastic DIP+ SOIC Package+	750 500	mW
P_D	Dissipation per Output Transistor	100	mW
Tstg	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.
+Derating - Plastic DIP: - 10 mW/°C from 65° to 125°C
SOIC Package: : - 7 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	3.0	18	V
V_{IN}, V_{OUT}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	-55	+125	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range GND≤(V_{IN} or V_{OUT})≤V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC ELECTRICAL CHARACTERISTICS(Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				≥-55°C	25°C	≤125 °C	
V_{IH}	Minimum High-Level Input Voltage	V_{OUT}=0.5 V V_{OUT}=1 V V_{OUT}=1.5	5.0 10 15	3.5 7 11	3.5 7 11	3.5 7 11	V
V_{IL}	Maximum Low - Level Input Voltage	V_{OUT}= V_{CC} - 0.5V V_{OUT}= V_{CC} - 1.0 V V_{OUT}= V_{CC} - 1.5V	5.0 10 15	1.5 3 4	1.5 3 4	1.5 3 4	V
V_{OH}	Minimum High-Level Output Voltage	V_{IN}=GND	5.0 10 15	4.95 9.95 14.95	4.95 9.95 14.95	4.95 9.95 14.95	V
V_{OL}	Maximum Low-Level Output Voltage	V_{IN}= V_{CC}	5.0 10 15	0.05 0.05 0.05	0.05 0.05 0.05	0.05 0.05 0.05	V
I_{IN}	Maximum Input Leakage Current	V_{IN}= GND or V_{CC}	18	±0.1	±0.1	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	V_{IN}= GND or V_{CC}	5.0 10 15 20	1 2 4 20	1 2 4 20	30 60 120 600	μA
I_{OL}	Minimum Output Low (Sink) Current	V_{IN}= GND or V_{CC} U_{OL}=0.4 V U_{OL}=0.5 V U_{OL}=1.5 V	 5.0 10 15	 3.84 9.6 25.2	 3.06 7.8 20.4	 2.16 5.4 14.4	mA
I_{OH}	Minimum Output High (Source) Current	V_{IN}= GND or V_{CC} U_{OH}=2.5 V U_{OH}=4.6 V U_{OH}=9.5 V U_{OH}=13.5 V	 5.0 5.0 10 15	 -2 -0.64 -1.6 -4.2	 -1.6 -0.51 -1.3 -3.4	 -1.15 -0.36 -0.9 -2.4	mA
I_{OZ}	Maximum Tree-State Leakage Current	Output in High-Impedance State V_{IN}= GND or V_{CC} V_{OUT}= GND or V_{CC}	18	±0.4	±0.4	±12	μA

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, R_L=200kΩ unless otherwise specified, Input t_r=t_f=20 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			≥-55 °C	25°C	≤125 °C	
t_{PHL}	Maximum Propagation Delay, Input A or Direction to Output Y (Figure 1)	5.0 10 15	270 120 80	270 120 80	540 240 160	ns
t_{PLH}	Maximum Propagation Delay, Input A or Direction to Output Y (Figure 1)	5.0 10 15	380 180 130	380 180 130	760 360 260	ns
t_{PHZ}	Maximum Propagation Delay, Output Enable to Output Y (Figure 2) R_L = 1 kΩ	5.0 10 15	120 80 60	120 80 60	240 160 120	ns
t_{PZH}	Maximum Propagation Delay, Output Enable to Output Y (Figure 2) R_L = 1 kΩ	5.0 10 15	220 100 80	220 100 80	440 200 160	ns
t_{PLZ}	Maximum Propagation Delay, Output Enable to Output Y (Figure 2) R_L = 1 kΩ	5.0 10 15	250 130 110	250 130 110	500 260 220	ns
t_{PZL}	Maximum Propagation Delay, Output Enable to Output Y (Figure 2) R_L = 1 kΩ	5.0 10 15	250 110 80	250 110 80	500 220 160	ns
t_{TLH}	Maximum Output Transition Time, Any Output (Figure 1)	5.0 10 15	200 100 80	200 100 80	400 200 160	ns
t_{THL}	Maximum Output Transition Time, Any Output (Figure 1)	5.0 10 15	120 60 40	120 60 40	240 120 80	ns
C_{IN}	Maximum Input Capacitance	-		7.5		pF
C_{OUT}	Maximum Tree-State Output Capacitance (Output in High-Impedance State)	-		15		pF

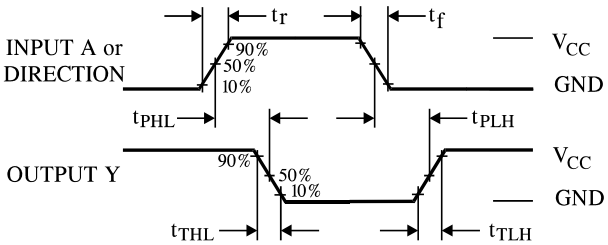


Figure 1. Switching Waveforms

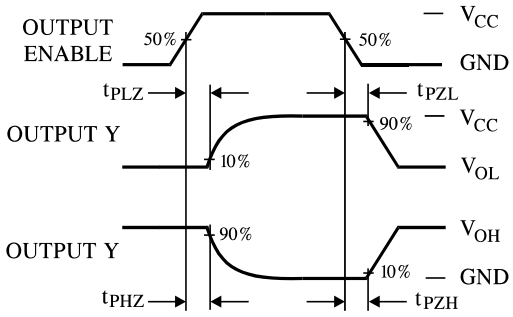
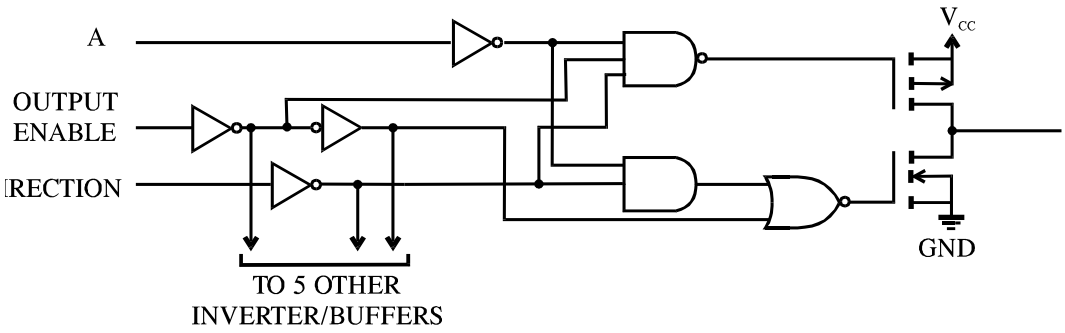


Figure 2. Switching Waveforms

EXPANDED LOGIC DIAGRAM
(1/6 of the Device)



INTEGRAL