

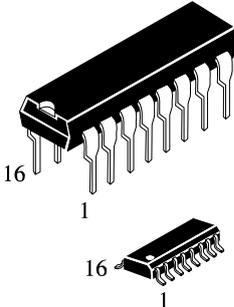
**IN74HC192**

**Presettable BCD/Decade UP/DOWN Counter**  
**High-Performance Silicon-Gate CMOS**

The IN74HC192 is identical in pinout to the LS/ALS192. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LS/ALSTTL outputs.

The counter has two separate clock inputs, a Count Up Clock and Count Down Clock inputs. The direction of counting is determined by which input is clocked. The outputs change state synchronous with the LOW-to-HIGH transitions on the clock inputs. This counter may be preset by entering the desired data on the P0, P1, P2, P3 input. When the Parallel Load input is taken low the data is loaded independently of either clock input. This feature allows the counters to be used as divide-by-n by modifying the count length with the preset inputs. In addition the counter can also be cleared. This is accomplished by inputting a high on the Master Reset input. All 4 internal stages are set to low independently of either clock input. Both a Terminal Count Down (TC<sub>D</sub>) and Terminal Count Up (TC<sub>U</sub>) Outputs are provided to enable cascading of both up and down counting functions. The TC<sub>D</sub> output produces a negative going pulse when the counter underflows and TC<sub>U</sub> outputs a pulse when the counter overflows. The counter can be cascaded by connecting the TC<sub>U</sub> and TC<sub>D</sub> outputs of one device to the Count Up Clock and Count Down Clock inputs, respectively, of the next device.

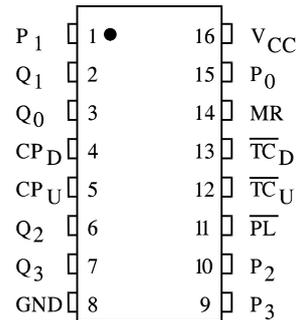
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0 μA
- High Noise Immunity Characteristic of CMOS Devices



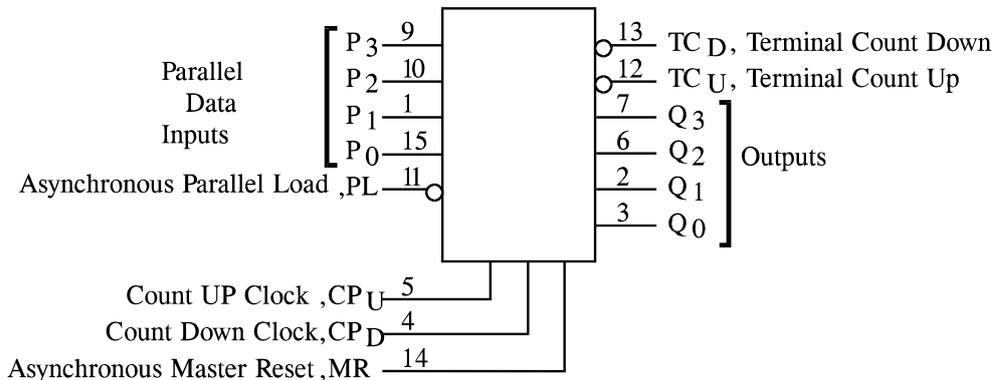
N SUFFIX PLASTIC  
 D SUFFIX SOIC

**ORDERING INFORMATION**  
 IN74HC192N Plastic  
 IN74HC192D SOIC  
 T<sub>A</sub> = -55° to 125° C for all packages

**PIN ASSIGNMENT**



**LOGIC DIAGRAM**



PIN 16 = V<sub>CC</sub>  
 PIN 8 = GND

**MAXIMUM RATINGS\***

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V <sub>IN</sub>	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	V
V <sub>OUT</sub>	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
I <sub>IN</sub>	DC Input Current, per Pin	±20	mA
I <sub>OUT</sub>	DC Output Current, per Pin	±25	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	±50	mA
P <sub>D</sub>	Power Dissipation in Still Air, Plastic DIP+ SOIC Package +	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

+Derating - Plastic DIP: - 10 mW/°C from 65° to 125°C  
SOIC Package: : - 7 mW/°C from 65° to 125°C

**RECOMMENDED OPERATING CONDITIONS**

Symbol	Parameter	Min	Max	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V <sub>IN</sub> , V <sub>OUT</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	V <sub>CC</sub>	V
T <sub>A</sub>	Operating Temperature, All Package Types	-55	+125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)			
	V <sub>CC</sub> = 2.0 V	0	1000	ns
	V <sub>CC</sub> = 4.5 V	0	500	
	V <sub>CC</sub> = 6.0 V	0	400	

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>IN</sub> and V<sub>OUT</sub> should be constrained to the range GND ≤ (V<sub>IN</sub> or V<sub>OUT</sub>) ≤ V<sub>CC</sub>.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

**DC ELECTRICAL CHARACTERISTICS**(Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				25 °C to -55°C	≤85 °C	≤125 °C	
V <sub>IH</sub>	Minimum High-Level Input Voltage	V <sub>OUT</sub> =0.1 V or V <sub>CC</sub> -0.1 V   I <sub>OUT</sub>   ≤ 20 μA	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V <sub>IL</sub>	Maximum Low - Level Input Voltage	V <sub>OUT</sub> =0.1 V or V <sub>CC</sub> -0.1 V   I <sub>OUT</sub>   ≤ 20 μA	2.0	0.3	0.3	0.3	V
			4.5	0.9	0.9	0.9	
			6.0	1.2	1.2	1.2	
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub>   I <sub>OUT</sub>   ≤ 20 μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
		6.0	5.9	5.9	5.9		
		V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub>   I <sub>OUT</sub>   ≤ 4.0 mA   I <sub>OUT</sub>   ≤ 5.2 mA	4.5	3.98	3.84	3.7	
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub>   I <sub>OUT</sub>   ≤ 20 μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
		6.0	0.1	0.1	0.1		
		V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub>   I <sub>OUT</sub>   ≤ 4.0 mA   I <sub>OUT</sub>   ≤ 5.2 mA	4.5	0.26	0.33	0.4	
I <sub>IN</sub>	Maximum Input Leakage Current	V <sub>IN</sub> =V <sub>CC</sub> or GND	6.0	±0.1	±1.0	±1.0	μA
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA	6.0	8.0	80	160	μA

**FUNCTION TABLE**

Inputs				Mode
MR	PL	CP <sub>U</sub>	CP <sub>D</sub>	
H	X	X	X	Reset(Asyn.)
L	L	X	X	Preset(Asyn.)
L	H		H	No Count
L	H		H	Count Up
L	H	H		Count Down
L	H	H		No Count

X = don't care

The IN74HC192 can be preset to any state, but will not count beyond 9. If preset to state 10, 11, 12, 13, 14 or 15, it will follow the sequence 10, 11, 12, 13, 4: 14, 15, 2 if counting Up, and follow the sequence 15, 14, 13, 12, 11, 10, 9 if counting Down.

Logic equations

For Terminal Count:

$$TC_U = Q_0 \cdot Q_3 \cdot CP_U$$

$$TC_D = \overline{Q_0} \cdot \overline{Q_1} \cdot \overline{Q_2} \cdot \overline{Q_3} \cdot \overline{CP_D}$$

**AC ELECTRICAL CHARACTERISTICS**( $C_L=50pF$ , Input  $t_r=t_f=6.0$  ns)

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			25 °C to -55°C	≤85°C	≤125°C	
f <sub>max</sub>	Minimum Clock Frequency (50% Duty Cycle) (Figures 1 and 6)	2.0	12	3.2	2.6	MHz
		4.5	36	16	13	
		6.0	43	19	15	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Clock to Q (Figures 1 and 6)	2.0	215	270	325	ns
		4.5	43	54	65	
		6.0	37	46	55	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, $\overline{PL}$ to Q (Figures 3 and 6)	2.0	215	270	325	ns
		4.5	43	54	65	
		6.0	37	46	55	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Clock to Terminal Count (Figures 2 and 6)	2.0	125	155	190	ns
		4.5	25	31	38	
		6.0	21	26	32	
t <sub>TLH</sub> , t <sub>THL</sub>	Maximum Output Transition Time, Any Output (Figures 1 and 6)	2.0	75	95	110	ns
		4.5	15	20	23	
		6.0	13	18	20	
C <sub>IN</sub>	Maximum Input Capacitance	-	10	10	10	pF

C <sub>PD</sub>	Power Dissipation Capacitance (Per Package)	Typical @25°C, V <sub>CC</sub> =5.0 V			pF
	Used to determine the no-load dynamic power consumption: $P_D=C_{PD}V_{CC}^2f+I_{CC}V_{CC}$	60			

**TIMING REQUIREMENTS**( $C_L=50pF$ , Input  $t_r=t_f=6.0$  ns)

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			25 °C to -55°C	≤85°C	≤125°C	
t <sub>su</sub>	Minimum Setup Time, Pn to $\overline{PL}$ (Figure 4)	2.0	100	125	150	ns
		4.5	20	35	30	
		6.0	18	22	26	
t <sub>h</sub>	Minimum Hold Time, Pn to $\overline{PL}$ (Figure 4)	2.0	0	0	0	ns
		4.5	0	0	0	
		6.0	0	0	0	
t <sub>w</sub>	Minimum Pulse Width, Clock (Figure 1)	2.0	150	190	225	ns
		4.5	30	38	45	
		6.0	26	33	38	
t <sub>w</sub>	Minimum Pulse Width, $\overline{PL}$ (Figure 3)	2.0	100	125	150	ns
		4.5	20	25	30	
		6.0	17	26	26	
t <sub>w</sub>	Minimum Pulse Width, MR (Figure 5)	2.0	100	125	150	ns
		4.5	20	25	30	
		6.0	17	26	26	
t <sub>r</sub> , t <sub>f</sub>	Minimum Input Rise and Fall Times (Figure 1)	2.0	100	100	100	ns
		4.5	500	500	500	
		6.0	400	400	400	

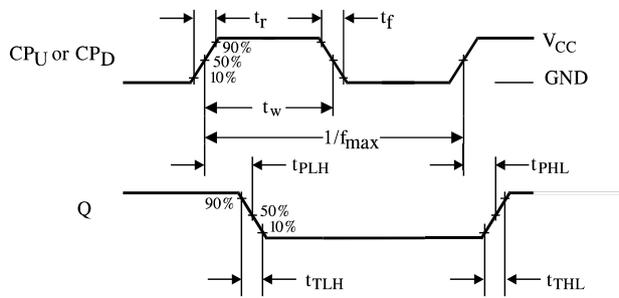


Figure 1. Switching Waveforms

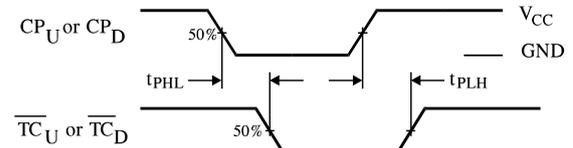


Figure 2. Switching Waveforms

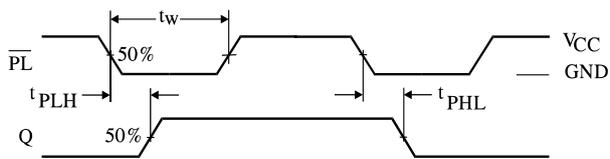


Figure 3. Switching Waveforms

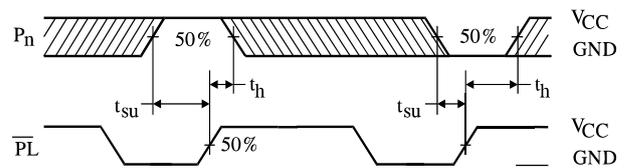


Figure 4. Switching Waveforms

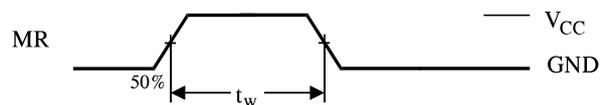
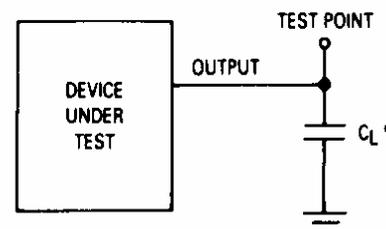


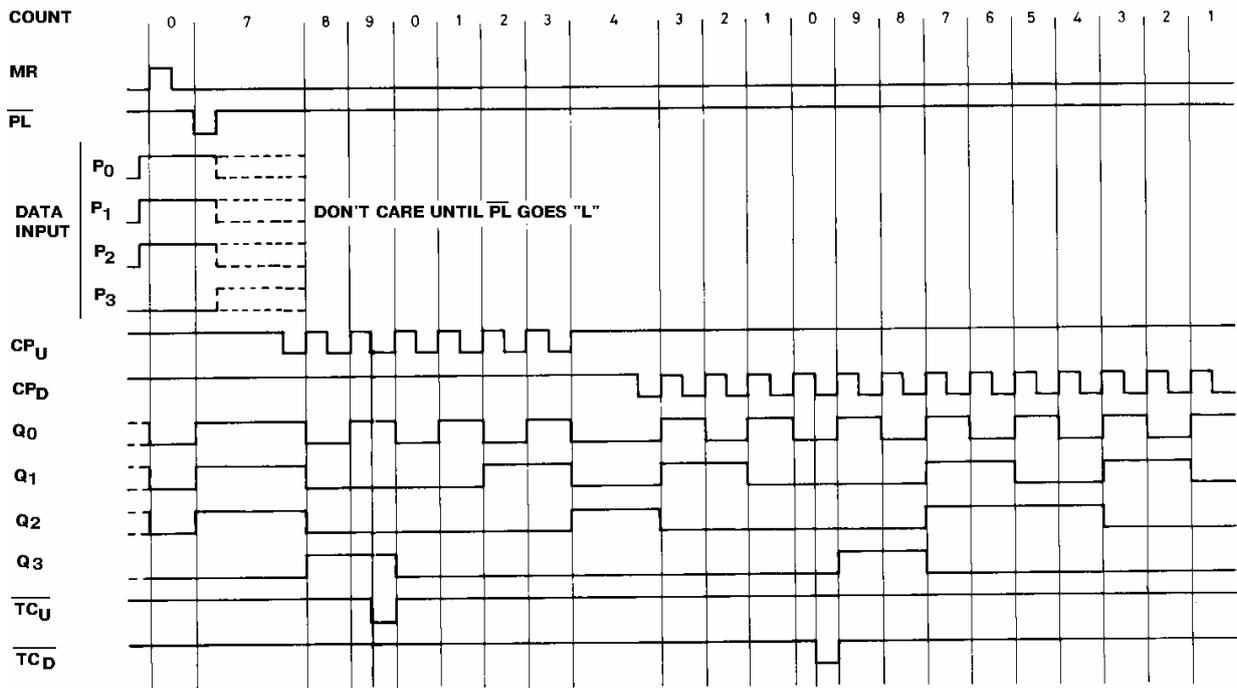
Figure 5. Switching Waveforms



\*Includes all probe and jig capacitance.

Figure 6. Test Circuit

TIMING DIAGRAM



EXPANDED LOGIC DIAGRAM

