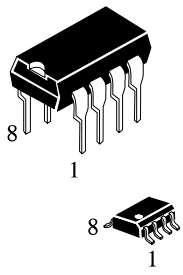
# IL34119

## LOW POWER AUDIO AMPLIFIER

The IL34119 is a low power audio amplifier integrated circuit intended (primarily) for telephone applications, such as in speakerphones. It provides differential speaker outputs to maximize output swing at low supply voltages (2.0 volts minimum). Coupling capacitors to the speaker are not required. Open loop gain is 80 dB, and the closed loop gain is set with two external resistors. A Chip Disable pin permits powering down and/or muting the input signal. The IL34119 is available in a standard 8 pin DIP or a surface mount package.

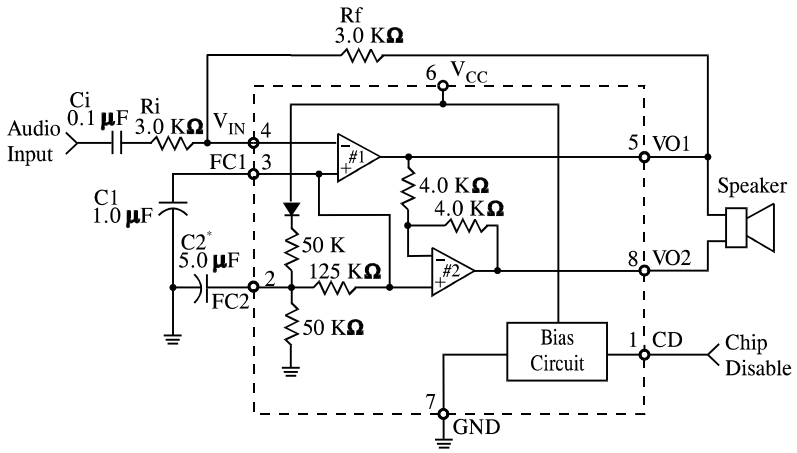
- Wide Operating Supply Voltage Range (2-16 Volts) - Allows Telephone Line Powered Applications
- Low Quiescent Supply Current for Battery Powered Applications
- Chip Disable Input to Power Down the IC
- Low Power Down Quiescent Current
- Drives a Wide Range of Speaker Loads (8-100Ω)
- Output Power Exceeds 250 mW with 32Ω Speaker
- Low Total Harmonic Distortion
- Gain Adjustable from <0 dB to >46 dB for Voice Band
- Requires Few External Components



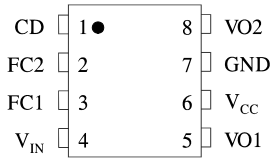

**ORDERING INFORMATION**

IL34119N Plastic
IL34119D SOIC
$T_A$ = -10° to 70° C for all packages

**SIMPLIFIED BLOCK DIAGRAM**




**PIN ASSIGNMENT**






INTEGRAL

**PIN DESCRIPTION**

| Pin | Symbol | Description |
|---|---|---|
| 1 | CD | Chip Disable - Digital input. A Logic "0" (<0.8 V) sets normal operation. A Logic "1" (≥2.0 V) sets the power down mode. Input impedance is nominally 90 KΩ. |
| 2 | FC2 | A capacitor at this pin increases power supply rejection, and affects turn-on time. This pin can be left open if the capacitor at FC1 is sufficient. |
| 3 | FC1 | Analog Ground for the amplifiers. A 1.0 μF capacitor at this pin (with a 5.0 μF capacitor at Pin 2) provides 52 dB of power supply rejection. Turn-on time of the circuit is affected by the capacitor on this pin. This pin can be used as an alternate input. |
| 4 | $V_{IN}$ | Amplifier input. The input capacitor and resistor set low frequency rolloff and input impedance. The feedback resistor is connected to this pin and VO1. |
| 5 | VO1 | Amplifier Output #1. The dc level is ≈ ($V_{CC}$ - 0.7 V)/2. |
| 6 | $V_{CC}$ | DC supply voltage (+2.0 to +16 Volts) is applied to this pin. |
| 7 | GND | Ground pin for the entire circuit. |
| 8 | VO2 | Amplifier Output #2. This signal is equal in amplitude, but 180° out of phase with that at VO1. The dc level is ≈ ($V_{CC}$ - 0.7 V)/2. |

**RECOMMENDED OPERATING CONDITIONS**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | 2.0 | 16 | V |
| $R_L$ | Load Impedance | 8.0 | 100 | Ω |
| $I_L$ | Peak Load Current | - | 200 | mA |
| AVD | Differential Gain (5.0 KHz bandwidth) | 0 | 46 | dB |
| VCD | Voltage @ CD (Pin 1) | 0 | $V_{CC}$ | V |
| $T_A$ | Operating Temperature, All Pakage Types | -10 | +70 | °C |

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, $V_{IN}$ and $V_{OUT}$ should be constrained to the range GND≤($V_{IN}$ or $V_{OUT}$)≤$V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or $V_{CC}$). Unused outputs must be left open.

**ELECTRICAL CHARACTERISTICS**($T_A$ = -10 to +70°C, $V_{CD}$ = 0 V)

| Symbol | Parameter | Test Conditions | Guaranteed Limits | | Unit |
|---|---|---|---|---|---|
| | | | Min | Max | |
| **AMPLIFIERS (DC CHARACTERISTICS)** | | | | | |
| $V_O$ | Output DC Level (VO1, VO2) | $V_{CC}$ =3.0 V, $R_L$ =16Ω<br>$R_f$ = 75 KΩ | 0.75 | 1.75 | V |
| $V_{OH}$ | Output High Level | $I_{OUT}$ = -75 mA, $V_{CC}$ = 2.0 V | 0.5 | - | V |
| $V_{OL}$ | Output Low Level | $I_{OUT}$ = 75 mA,<br>2.0 V ≤ $V_{CC}$ ≤ 16 V | - | 0.55 | V |
| $\Delta V_O$ | Output DC Offset Voltage (VO1-VO2) | $V_{CC}$ =6.0 V, $R_L$ =32Ω<br>$R_f$ = 75 kΩ | -200 | 200 | mV |
| $I_{IB}$ | Input Bias Current @ VIN | $V_{CC}$ =6.0 V | - | 1600 | nA |
| $R_{FC1}$ | Equivalent Resistance @ FC1 | $V_{CC}$ = 6.0 V | 100 | 220 | KΩ |
| $R_{FC2}$ | Equivalent Resistance @ FC2 | $V_{CC}$ = 6.0 V | 18 | 40 | KΩ |
| $V_{IH}$ | Minimum High-Level Input Voltage | | 2.0 | - | V |
| $V_{IL}$ | Maximum Low-Level Input Voltage | | - | 0.8 | V |
| $R_{CD}$ | Input Resistance | $V_{CC}$ = $V_{CD}$ = 16 V | 50* | 175* | KΩ |
| **AMPLIFIERS (AC CHARACTERISTICS)** | | | | | |
| $r_i$ | AC Input Resistance ($V_{IN}$) | | 22.5 | - | MΩ |
| $A_{VOL1}$ | Open Loop Gain (Amplifier #1) | f = 100 Hz, $V_{CC}$ = 6.0 V,<br>$V_{FC2}$ = 2.65 V | 60 | - | dB |
| $A_{V2}$ | Closed Loop Gain (Amplifier #2) | f = 1.0 KHz, $V_{CC}$ = 6.0 V,<br>$R_L$=32 Ω | -0.35 | +0.35 | dB |
| GBW | Gain Bandwidth Product | | 1.125 | - | MHz |
| $P_{OUT3}$<br>$P_{OUT12}$ | Output Power | $V_{CC}$ = 3.0 V, $R_L$ = 16 Ω,<br>THD ≤ 10%, $V_{FC2}$ = 1.15 V<br>$V_{CC}$ = 12.0 V, $R_L$ = 100 Ω,<br>THD ≤ 10%, $V_{FC2}$=12 V | 55<br>400* | -<br>- | mW |
| THD | Total Harmonic Distortion | $V_{CC}$ = 6.0 V, $R_L$ = 32 Ω,<br>f = 1.0 KHz, $P_{OUT}$ = 125 mW | - | 5.0 | % |
| PSRR | Power Supply Rejection | $V_{CC}$ = 6.0 V, $\Delta V_{CC}$ = 3.0 V,<br>C1 =∞, C2 = 0.01 μF | 35 | - | dB |
| GMT | Muting | $V_{CC}$ = 6.0 V, f = 1.0 kHz,<br>CD = 2.0 V | 50 | - | dB |
| **POWER SUPPLY** | | | | | |
| $I_{CC1}$<br>$I_{CC2}$ | Maximum Power Supply Current | $V_{CC}$ =3.0 V, $R_L$ =∞,CD=0.8V<br>$V_{CC}$ =3.0 V, $R_L$ =∞,CD=2.0V | -<br>- | 5.0<br>125 | mA<br>μA |